form referred to as high-fidelity netlist, in which a board containing the discrete parts constituting the MCM is built with as close to identical a netlist as possible. The board is socketed for system insertion. Only after functional verification is achieved with the "high-fidelity netlist" is the design released for fabrication. After fabrication, the resulting MCM is temporarily socketed into a board identical in size and fixturing to the high-fidelity netlist format. The MCM is then inserted interchangeably and functionally verified. The procedure of high-fidelity verification is recursed as necessary in more complex approaches, such as 3D-MCM stacks. The high-fidelity netlist is not without drawbacks, particularly in die-optimized cases where fixturing access is difficult or impossible because of the severe differences in parasitic capacitance. Another pitfall that often occurs in schedule-pressured development programs is the temptation to "shot-gun," that is, to attempt to verify breadboards while the MCM is in design (or worse, fabrication).

8.3.4.4 Putting the "Play" into Plug and Play

The vision of plug and play epitomizes an effective open-systems approach, since it employs a number of open-systems standards in a synergistic manner to achieve interchangeability and interoperability. The plug-and-play concept is familiar as a result of the attention it has received from recent attempts to improve hardware interchangeability in PC hardware. The results of these attempts have been the formation of a set of industry specifications.[118] Despite these specifications, which were built upon physical (connector), electrical (e.g., 5 V / 3.3 V), logical (high-performance, low-power CMOS), software characteristics (drivers layered onto a standard operating system), many early industry attempts to achieve plug and play were problematic, leading in some cases to the less flattering descriptor, plug-and-pray.

Nevertheless, the plug-and-play concept is clearly the highest and most desirable level of open-systems implementation. In the limit argument, a true plug-and-play system would require no hardware bridges, fixes, or software patches, and it would adapt to integrate, in real time, with theoretically unknown assets if strict compliance to the appropriate plug-and-play specification were achieved. Unfortunately, by the same token, plug and play is one of the most abused descriptors used to advertise or market components and even subsystems. Often wide-ranging applicability is confused with the real ability to achieve plug and play.

8.4 Advanced Approaches

This section examines the following advanced approaches to packaging.

- Some extensions of packaging boundaries presented through case studies and techniques
- An advanced 3D packaging system that embodies a fresh look at packaging: the Highly Integrated Packaging and Processing (HIPP) program is developing this concept, one that seems to address the key issues of both micro- and high-performance systems.
- A hypothetical third-generation in MCM packaging
- An approach to remove many boundaries in packaging, multifunctional structures (MFS)

8.4.1 Extending the Boundaries that Define Packaging

Three broad approaches exist for engineering a system of packaging. The first is to simply use available technologies, such as to order from a catalog or do commodity-oriented practices, such as printed circuit board or cofired ceramic substrate design. The approach is safe albeit limited in the potential benefits accrued. The second approach involves localized optimizations, such as engineering a system element for a preexisting system in which only the new element can receive benefit of advanced packaging engineering. The final approach, reminiscent of a system-on-a-chip philosophy, encourages reviewing a large piece of a system, perhaps several subsystems, for exploitative opportunities in package engineering.

In the latter cases we have the opportunity to extend the boundaries of packaging, and not necessarily force a rote procedure. We begin considering some possibilities by first reviewing two case studies in HDI packaging, followed by a discussion on some techniques applicable to high-performance microinstruments.

8.4.1.1 Case Studies in High Density Interconnect

8.4.1.1.1 Radiation-Hardened HDI Space Computer (RHSC)

Type of Design. Stand-alone ruggedized general-purpose computer. The RHSC CPU (central processor unit) was based on the Lockheed-Martin rad-hard 1750A, and the design contained a collection of radiation components from many other vendors representing a component cost well in excess of $100,000/module, making the RHSC one of the most costly MCMs based on component cost alone. The RHSC design is unique in its capability to operate in nuclear radiation environments without upsetting real-time operation and without loss of data.

Radiation-hardened implementation contained, besides a dual lock-step 1750A microprocessor, several megabits of main memory and special-purpose integrated circuits for memory management, data protection, and system control. Though seemingly simple compared with advanced commercial microprocessors, the RHSC is designed to provide military space platforms with a survivable computer in the minimum size, weight, and power possible. In its form, the system replaces a 10.8-lb computer while providing dramatically improved robustness from the implementation of an operate-through approach that protects critical data and real-time operation from upset in a nuclear environment. Traditional practices for space systems require hermetic assemblies because of concerns of reliability degradation from long-term moisture permeation and the outgassing products of hybrids and MCMs affecting other sensitive instruments in space systems.

Advanced Packaging Technology Used

- Large format, complex digital MCM system 3.8 × 2.5 in., >500 I/Os, 12.3 W, hermetic assembly
- HDI patterned overlay MCM substrates
- HDI subtile construction (planar MCM inset within another planar MCM)
- 3D, edge-interconnected stacking methodology

In the RHSC, the HDI process was exploited in new ways, as shown in Fig. 8.38. For example, a minimodule (1.4 in. sq) containing the 1750A processor was fabricated, separately tested, and inset within a larger substrate as an HDI subtile component. As in the case of individual components, the minimodule was also placed into a larger, planarizing substrate with dozens of other integrated circuits and passive components. This compound MCM was then subsequently integrated into a stacked ensemble of two identically sized substrates using the 3D extension of the patterned overlay process. Photographs of the RHSC before and after insertion of the subtile are shown in Fig. 8.39. The complete construction of the very compact RHSC system involved no fewer than five multilayer copper-kapton interconnect systems, as shown in Fig. 8.38.

The 3D RHSC system required hermetic assembly into a package; the associated structures are depicted in Fig. 8.40. The special package developed involved a series of highly dense multilayer ceramic (MLC) inserts, placed within a kovar enclosure. MLCs were used in the RHSC because of the tight pitch (<50 mils precludes the use of the more traditional glass beads). The kovar can was designed to permit wire-bonding from lands on the top substrate to an inner bond shelf formed by the MLC inserts. After wire-bonding, the RHSC package was sealed with a lid through a standard seam-welding process, forming the desired hermetic enclosure.

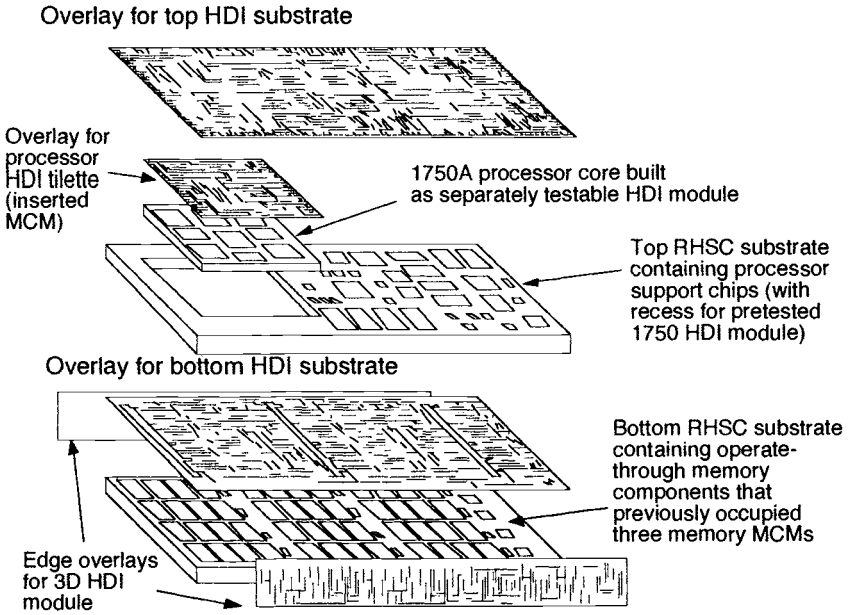

Fig. 8.38. Exploded view of an RHSC module, illustrating the use of HDI subtiles and 3D assembly.

Fig. 8.39. RHSC processor substrate, illustrating HDI subtile concept: (left) unpatterned substrate, (right) substrate with HDI subtile insert.

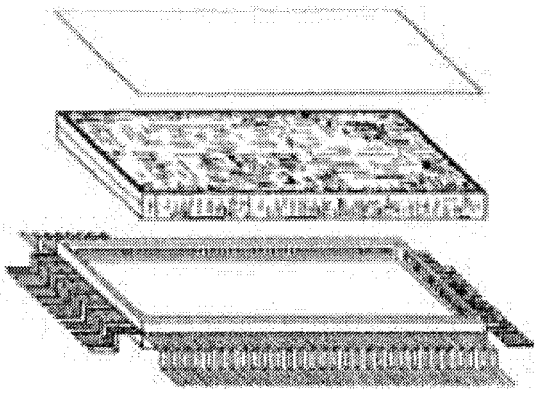

Fig. 8.40. 3D RHSC and associated hermetic package.

A Real Product or a Prototype for an MCM Technology? RHSC was built as a generic demonstration of advanced packaging and survivable computer technology for various U.S. Department of Defense applications and funded through the Defense Nuclear Agency. A limited number of prototypes were built successfully as a proof-of-principle demonstration. The design was proven in brassboard form prior to MCM design in high-radiation environment tests. The MCM itself was specially developed. The fabrication and initial demonstration were in spring 1994.

Unique Design Features. RHSC represents one of the most complex MCM systems built to date. It examined new forms of HDI, the integration of large MCM form factors in 3D form, the unique provisions/requirements of HDI MCM construction with subtiles, the trade-offs (electrical, thermal, mechanical) of a 3D MCM, the merging of IC components from a number of disparate suppliers, known-good-die, and known-good-module.

Lessons Learned

- PROM components locked into substrate were impacted by later software changes.
- Partition of the design was driven to two large substrates instead of four smaller substrates because of the I/O requirements, which drove the minimum perimeter size used in RHSC.
- Testing drove much of the I/O demand and most of the special features of the RHSC, especially the subtile configuration. A module-on-board approach facilitated testing each large substrate.
- The subtile was designed to drop into an existing package used by Lockheed Martin, simplifying functional test of unique ICs.

How an MCM Approach Benefited this Development. Space systems require maximal economy of launch weight and power consumption. The MCM implementation of the RHSC replaced large brassboards, which themselves contained one or more MCMs. The closest off-the-shelf correlating to the RHSC before it was designed was a 10.8-lb computer, which was less mechanically robust and would have been disrupted by nuclear environments through which the RHSC could have operated.

The key result of the RHSC project was to press the limits of integration and complexity for a specialized application, including large-format MCMs, compound MCMs, and 3D MCMs

8.4.1.1.2 Advanced Instrument Controller (AIC)

Type of Design. Stand-alone low-to-medium performance, general-purpose processor designed for radiation-tolerant operation, with versatile interface/operating options. The AIC block diagram, shown in Fig. 8.41, involves a tightly coupled processor-memory-analog interface-chip combination. Through a tightly coupled MCM design approach, the AIC achieves a 3 g, 1.0- × 1.4-in. form factor and a 50-mW-power budget, and is designed to operate in 30,000-G environments at operating temperatures down to −130°C. The AIC was developed under NASA/USAF funding for the Deep Space II interplanetary probes attached to the Mars 98 mission.

Advanced Packaging Technology Used

- Few-chip, mixed-signal MCM system (1.0 × 1.4 in., 120 I/Os, plastic assembly)
- Tightly-coupled MCM design
- Plastic HDI patterned overlay MCM substrates
- Surface-mount components for trimming end performance
- In situ reprogrammability of memory

Die-level interconnections for plastic HDI are as in the standard HDI patterned overlay process. In the AIC, modules are sawed apart after carriers containing 6, 8, or 12 modules each are fabricated (like IC wafers). Most surface-mount components are then mounted and soldered, and

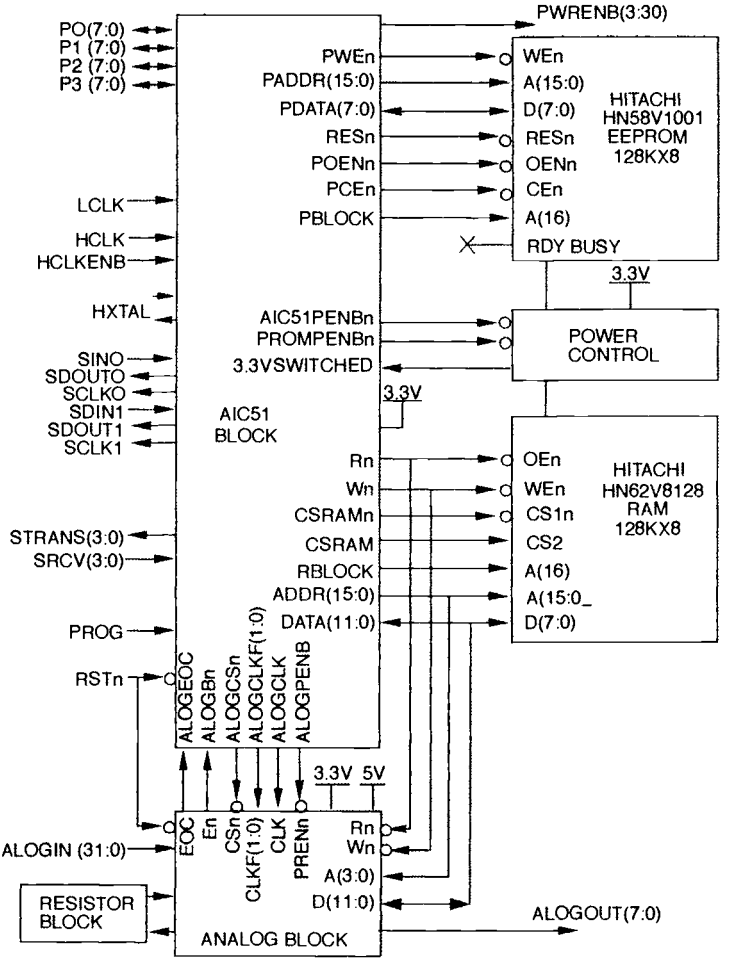

Fig. 8.41. Architecture of the AIC.

the balance are added after testing. In the initial modules built, modules were wire-bonded temporarily to small boards for evaluation, and then transferred to flight assemblies (e.g., another board), where wire-bonds are replaced by a flex-based lead attachment. Later generation AICs employ lead frames added during surface-mount attachment, which greatly reduces difficulty of testing and end use.

The AIC leaves hermetic assembly as an option, which has not been required by current users. The AIC can be placed within a kovar or ceramic package, if required, similar to traditional ICs and MCMs. AICs are being investigated for a number of applications with different end-packaging arrangements, ranging from using AIC as a subtile to fully enclosing the AIC within a small kovar package.

A Real Product or a Prototype for an MCM Technology? The AIC was an enabling application and provided a unique opportunity to do "intelligent things" with advanced concepts in plastic-based HDI technology. While ceramic HDI technology had received exposure to a number of flight projects, the plastic form of HDI had not been used in previous applications (since AIC, other flight experiments based on plastic HDI have been established). The appeal of the AIC, a

simple ultralow-power utility controller designed for space application, has not been limited to the original application. A number of other NASA and DOD programs are developing systems for flight with AICs or are evaluating AIC samples for potential use.

Unique Design Features

- CPU modified from an 8051 design
- 128 K × 8 SRAM and EEPROMs
- Analog application specific integrated circuit (ASIC)
- Large number of resistors bundled into a resistor-ASIC
- A p-channel FET, and other passive components

The AIC employs tightly coupled MCM design, which permits exploitation of

- Nonperipheral die area
- Smaller drivers on integrated circuits (sized for less than 10 pF drive)
- Large I/O between components within an MCM with relatively low I/O count
- Splicing in components from multiple processes

The AIC's CPU, for example, has more than 150 I/Os, while the MCM has only 120. The resistor ASIC reduced many fabrication uncertainties as well as design time for the analog ASIC, since the resistor values could be optimized independently, regardless of the sheet resistance values of the analog IC. The unwieldy number of resistors (~50) are absorbed within the MCM, freeing the user from the burden of more complex integration. In some applications, the AIC only needs applied voltage, as the collection of components (including even two oscillators) required for a minimal system are within the MCM. The AIC represents, therefore, a system-on-a-chip, albeit a relatively simple system. The ability of nonperipheral access was not exploited, however, as this was viewed as too traumatic a change in the current IC design/verification culture.

Some of the ICs used in the AIC are shown in Fig. 8.42. The CPU, built in the National Semiconductor 0.35-mm process, is obviously pad-limited [Fig. 8.42 (a)], based on the concentration of VLSI interconnect in the central region of the die. Had a distributed I/O array been used, the die size could have been substantially reduced. The CPU contains a barrage of user I/Os (including 32 discrete I/Os and 6 serial ports, along with a variety of power-management features and interfaces). Some of the interesting power-management features of the AIC include its ability to select from a palette of internal and user-provided oscillators and a separate copy of the entire data and address bus that is generated for the EEPROM (electrically erasable programmable read-only memory) to enable the AIC to physically remove power from the EEPROM when it is not in use without creating an undesired bus-loading condition for other components.

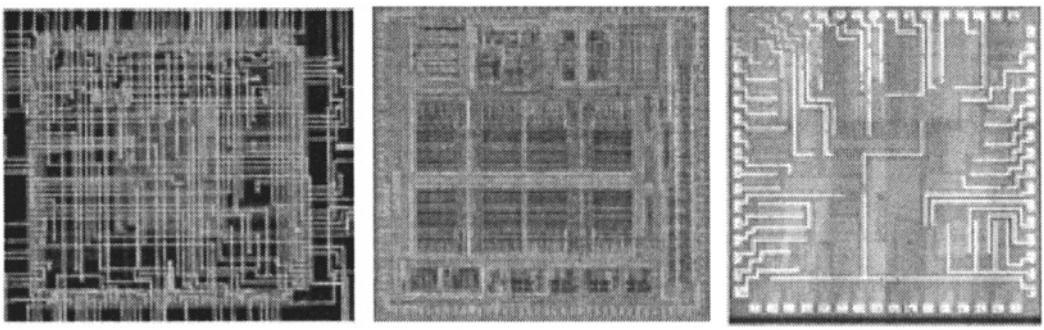

Fig. 8.42. Some of the ICs used in the AIC. (a) AIC51 CPU, shown here during an intermediate fabrication step (HDI traces visible over die and bond pads), (b) analog ASIC, (c) resistor ASIC.

The analog ASIC [Fig. 8.42 (b)] built in the Orbit Semiconductor 2-mm process contained approximately 70,000 components and implemented a surprising array of functions:

- 32 external A/D channels, 12-bit resolution
- 16 additional internal A/D channels, 12-bit resolution to monitor ASIC health and status
- 8 individually programmable DAC channels, 10-bit resolution (fed back to some of the internal A/D channels)
- Band-gap reference
- Proportional to absolute temperature (PTAT) thermal sensor

One of the most interesting features of the AIC is the in-situ reprogrammability of its program and data through one of the six AIC serial ports. The AIC, because of this feature, can be reprogrammed without disassembly. Furthermore, the AIC can literally be personalized with a variety of unique data, such as serial codes, calibration coefficients, even a reduced "traveler" containing process history. In the Deep Space II mission, the AIC is designed to function with discontinuous applied power, because of the high probability that the extreme cold will periodically render the battery temporarily nonfunctional. The AIC, by virtue of this capability, can display history-dependent behavior and be put to sleep for extended periods of time.

Lessons Learned

- The AIC did not exploit the ability to access nonperipheral bond pads on its ICs, which was fortunate at least at the time this decision was made, as it would have been difficult to pretest the die. The impacts of pretest (somewhat short of the KGD functional guarantee) can be profound, even with few-chip MCMs.
- At the time of this writing, the analog ASIC is not pretesting and is consequently the most common failure mode.
- Simple wafer probing of the CPU has kept the yield within tolerable bounds. Hence, tightly coupled approaches must be assessed carefully.
- It is believed that in time, a few-chip design can more advantageously exploit reduced drivers and nonperipheral distribution, in which case the MCM is viewed merely as a monolithic component.
- Similarly, the choice of a resistor ASIC was found to be much more costly than previously imagined. Newer versions of the AIC were designed without it, and a 75% cost savings and 12-week schedule savings were realized. This finding is disturbing, as the elimination of many passive components heuristically should reduce cost, indicating opportunities for improvement in the current component development infrastructure. Newer technologies with embedded passives could possibly be exploited.
- The most sobering impact that the tightly-coupled design has on a time-critical project is that it requires concatenation of the development of both the ASIC and the MCM, resulting in a very lengthy development cycle.
- In the AIC development, both the CPU and analog ASIC were first-pass successful, but the resistor ASIC and MCM were not. In the former case, no overall schedule impact was experienced, as the refabrication was effected while the CPU and analog ASIC were still in development. The MCM design error, however, resulted in a 4-month schedule impact. The schedule impact could have been doubled had the CPU contained flaws.
- The MCM design flaws, while preventable, were not caught by traditional tools.
- Conclusions are that while tackling both die and MCM designs, especially for a tightly coupled design, results in optimal size, weight, power, performance, and ultimately low recurring cost, the risks can be great. Mitigating this risk requires careful design and planning up front.

How an MCM Approach Benefited this Design. The MCM implementation of the AIC is shown in Fig. 8.43. AICs could not have been built without MCM technology. While not a high-performance device, the AIC represents a greater amount of silicon than a monolithic IC can accommodate, but not much greater. The use of MCM permits the independent optimization of separate components. For example, better EEPROMs in the future can replace the current ones, and enhancements can be phased in gradually. As monolithic silicon improves, the AIC can either shrink through the use of BGA/CSP approaches, or increase in functionality. When the current AIC can be rendered as a single chip, new AICs with added functionality will be realized such that the packaging remains just outside the realm of monolithic implementation. This is in direct contrast to the WSI research of the 1980s, in which WSI circuits could often be realized monolithically (with higher performance) during the horizon of a single project. On the other hand, designs such as AIC seem to offer the greatest possibility for success because they can stay just outside the reach of monolithic ICs.

The key result of the AIC project was to demonstrate the utility of a simple system-on-a-chip concept, made possible through a tightly coupled MCM design approach.

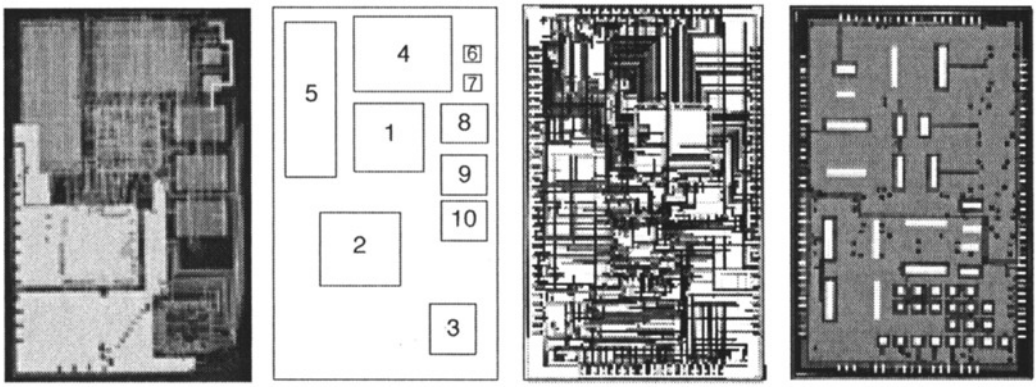

Fig. 8.43. AIC MCM. (a) AIC after first two levels of metallization; (b) legend: (1) CPU, (2) analog ASIC, (3) resistor ASIC, (4) 128 K × 8 EEPROM, (5) 128 K × 8 SRAM, (6–10) capacitors; (c) CAD files of some AIC metal and "drill" (via) layers; (d) AIC after HDI fabrication (components obscured by metallization and green solder mask coating).

8.4.1.2 Exploitation Techniques for Microinstrument Design

Just as a monolithic IC can be viewed as a synergistic arrangement of many individual transistors, microinstruments should be viewed as a synergistic arrangement of many individual components, not just electronics, but sensors and actuators. Sensors and actuators of an integrated microsystem correspond to the interface of physical domains, such as heat, light, sound,[119] radiation, and chemistry. This integration can be achieved monolithically or by hybridization, that is, the "magic of advanced packaging." Are aggressive miniaturization efforts always rewarding? It seems that in some cases physical size does scale and can accommodate miniaturization, but losses may not. The use of more sensitive physical effects may be required, or cleverer exploitations of designs pursued. Robustness is always desired, as it allows a greater diversity of operating conditions.

In this section, a few techniques that could be readily applied to constructing microinstruments are discussed. Constant-floor plan or quick-time reconfigurable designs allow more rapid mechanization of new concepts. Flex-based construction permits novel exploitation of flexible circuits to create 3D systems. Finally, some approaches for exploiting the high-performance nature of packaging to build better instruments are discussed.

8.4.1.2.1 Constant Floor Plan MCMs/Quick-time Reconfigurable Techniques

In a constant floor plan (CFP) MCM, preplaced components are arranged strategically in a substrate, but only partially interconnected, permitting an end user to complete the last stages of wiring and assembly for a particular application. The technique is particularly attractive in HDI processes, where a variety of components can be recessed within a substrate, leaving the entire module top surface available for adding components. The CFP MCM is a packaging analogy of a gate-array IC, where prefabricated transistor arrays are interconnected by completing the metallization system. The quick-time reconfigurable (QTR) approach is a variation on the CFP MCM in which a largely nonconnected MCM is programmed by adding a circuit board containing the final connection pattern and surface-mount components. In the QTR scheme, it is possible to exchange the circuit board quickly, creating a kind of plug-and-play system. QTR approaches are particularly convenient for complex sensors. The development of analog processing for a given sensor is necessarily custom because of the need to supply special timing, bias, amplification, and level-shifting networks for each variation. Furthermore, the resulting output signals vary in signal amplitude and format and have their own special timing relationships.

A conceptual example of a QTR system is shown in Fig. 8.44, involving a patterned overlay HDI module. Since patterned overlay MCMs feature planar surfaces, the introduction of a solder-bump array provides a compliant contact system for mounting a quickly customizable PWB. It is the introduction of the latter component that provides the QTR feature. Through custom patterning of commodity PWB technology (it is possible to fabricate them within 24 hours after transmittal of electronic design files), the final interconnection scheme is patterned, configuring bias, timing, filter, and amplification networks as needed for a given sensor. MEMS sensor and actuator arrays can also be implemented in a flexible and rapid manner. The use of semirigid flex PWBs also allows the integration of a final connector.

8.4.1.2.2 Flex-based Construction

In flexible circuitry, the "flatland" analogy of planar construction approaches can be, if not broken, at least bent. The example of a folded flexible MCM shown in Fig. 8.20(d) can be extended to many other concepts. For example, a three-axis inertial reference unit could be readily

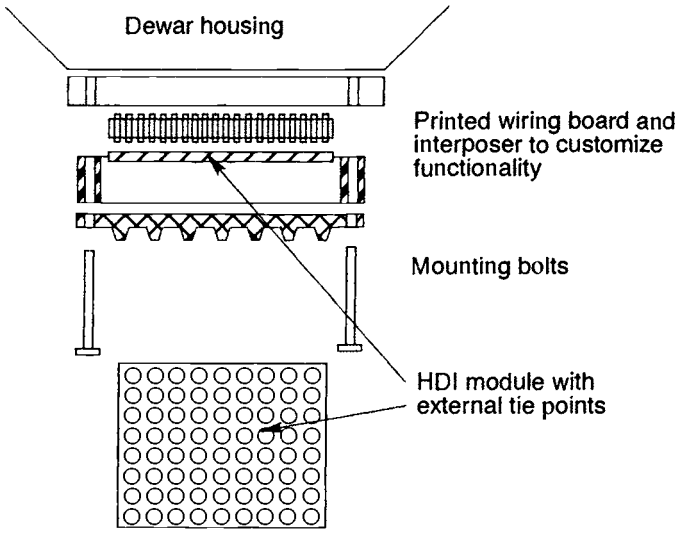

Fig. 8.44. QTR MCM.

constructed using a single-axis MEMS device built on three small MCMs, as shown in Fig. 8.45. The assembled MCM, fabricated as a continuous planar assembly, is readily converted into a three-axis system by folding the assembly like a box, around perhaps a "trueing" block, which could contain other electronics.

8.4.2 Highly Integrated Packaging and Processing

Traditional packaging hierarchy has, by comparison, seen little improvement because continual progress in feature size improvement of the IC takes pressure off striving for improvements. Most research in 3D packaging suffers from a lack of critical mass and applications pull, resulting in many impressive "hand-crafted" laboratory curios that lack acceptance. For the most part, 3D packaging research has centered around simple die stacks, with a considerable spread of substrate stacking approaches, most of which are implemented once with unclear benefit.

An AFRL initiative, referred to as the HIPP program, offers a fundamental reexamination of the packaging hierarchy and the successes and failures in 3D advanced packaging. In essence, it provides the implementation of a new hierarchy that complements the traditional one, but with important benefits to new technologies such as MCMs. The HIPP system offers a counterpoint to the inefficient frameworks in conventional packaging, which often cannot exploit the benefits of functions with multiple MCMs. Assemblies built in the HIPP approach can be merged into L2–L4 of the existing hierarchy whenever necessary and convenient. The HIPP framework, as an efficient MCM containment system, may not on the surface seem to achieve the impressive densities of laboratory-created 3D approaches. Spectacular gains of certain 3D approaches can be meaningless in complex system applications since those benefits cannot be accrued to the variety of component and circuit classes that make up an average system because of an intrinsic lack of "packaging services" needed in a complete system (e.g., thermal and electrical management). HIPP provides these services in a multitechnology framework, one that can allow any individual MCM to deliver the maximum benefit in most systems of reasonable complexity.

8.4.2.1 HIPP Assembly Structure

The HIPP program has sought packaging solutions more optimal at a system level, based on the concept of closely integrating a collection of various MCM substrates or other assemblies of identical size and conductor arrangement. Early artist concepts for these approaches are shown in Fig. 8.46. The first approach [Fig. 8.46(a)] involved the use of framed interposers and surface border interconnections, where contacts passed through entire substrates. Though efficient for bussed structures, this approach exacts a severe I/O penalty for complex substrate-to-substrate interconnections. For example, if the first substrate connects to the eighth with 80 signals, those 80 signals must be passed through substrates 2–7, whether or not those signals have a connection within

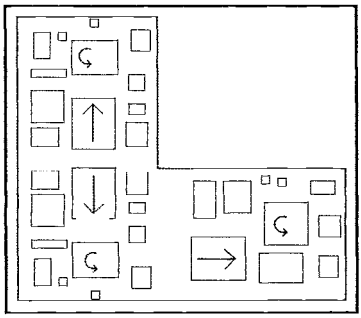

Fig. 8.45. Three-axis MCM built onto folded-flex HDI (shown before folding).

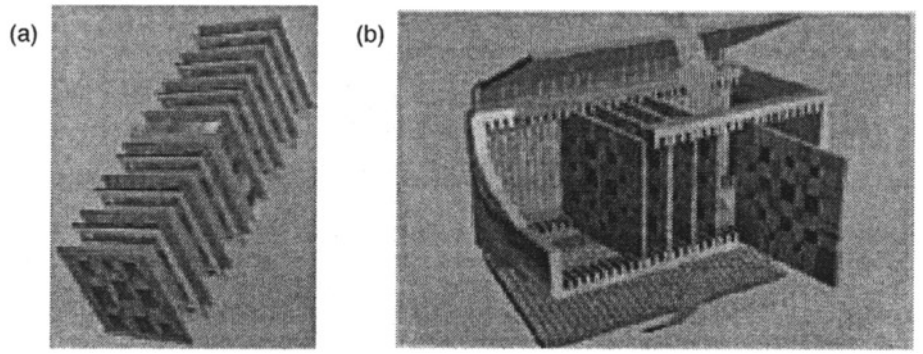

Fig. 8.46. Original HIPP concepts.

those substrates. At the random complexities represented by many heterogeneous systems, an unacceptably high amount of substrate real estate would be devoted to "pass-through" interconnect. The edge-interconnect system, shown in Fig. 8.46(b), provides an obviously more "agile" interconnection manifold, but requires tremendous edge-contact density on particular substrates, which could not be readily accommodated by the present state of the art (20–40 mils).

The requirements of candidate HIPP structures include:

- High I/O densities (up to 1000/layer)
- Heterogeneous signal composition (i.e., analog signals, digital, power, and microwave signals)
- Modularity and serviceability for layer repair and replacement
- Adequate power and thermal management
- Adequate I/O density at the second level of packaging
- Robustness for applications in harsh environments

Continued research led to a hybridization of the earlier conceptual approaches in which the theoretically high-contact densities of the first approach could be combined with the interconnection manifold agility of the second approach while addressing the basic requirements of a candidate heterogeneous 3D packaging system. Such a system, the baseline for a demonstration for the Discriminating Interceptor Technology Program (DITP), is shown in Fig. 8.47.

8.4.2.1.1 Segments

Figure 8.47 illustrates a many-layer 3D packaging approach that combines a number of segment entities into an assembly. The segments, which are the common and fundamental building blocks of HIPP, contain one or more MCMs or small circuit boards containing components. Systems, such as the DITP platform, can be partitioned into a number of segments, as shown in Fig. 8.47(a). In this case, the HIPP assembly baselined for DITP consists of approximately 16 segments (numbers reflect current order of segments from the front in the preliminary design):

- MSP (malleable signal processor) Subsystem 1
  - Sensor adaptation segment for passive focal-plane array sensor (2)
  - MSP 0.5 core segment (4)
  - MMGT (MSP management) segment, which contains MSP management processor and FI32 interface (5)
- MSP Subsystem 2
  - Ladar (light-based [laser] radar) adaptation segment containing nondigital interface (level shifters) (3)
  - MSP 0.5 core segment (6)
  - MMGT segment for second MSP core (7)

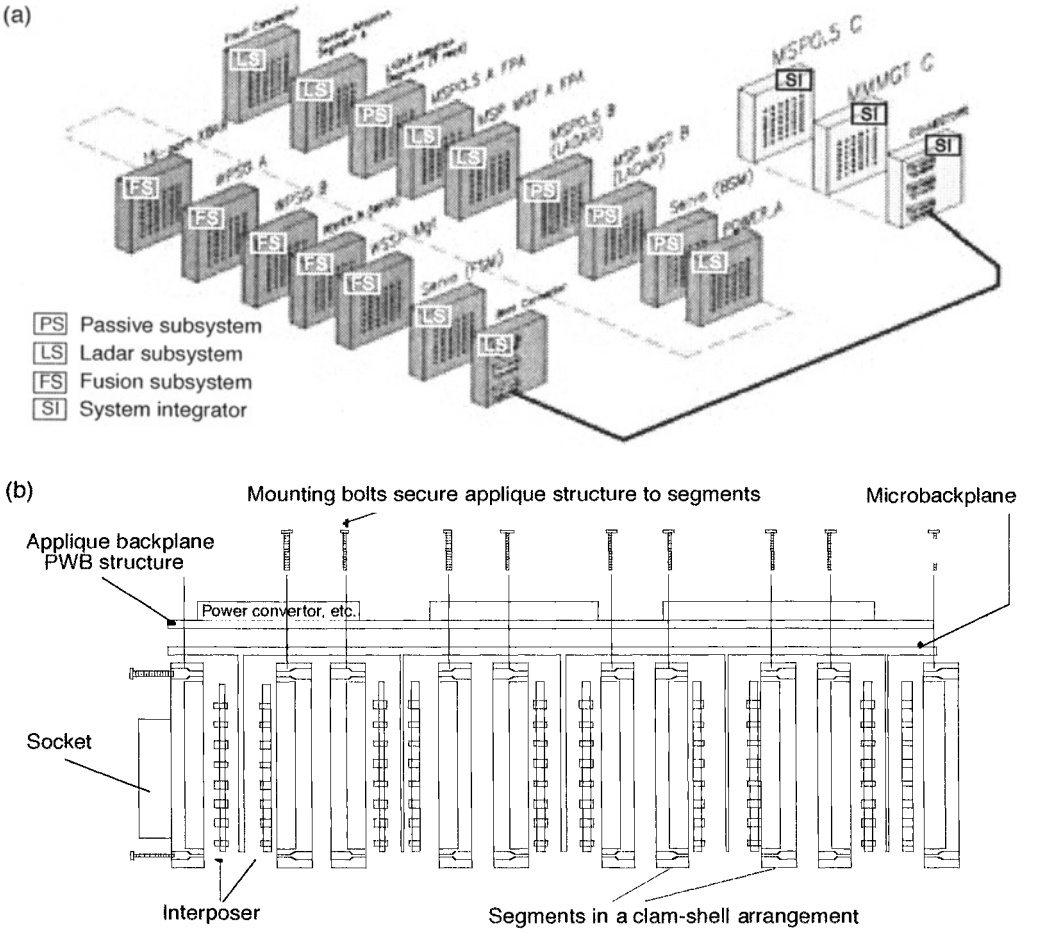

Fig. 8.47. HIPP baseline concept for DITP. (a) simplified physical representation (telemetry function external to sensor and fusion engine), (b) more detailed drawing illustrating interconnect features.

- Fusion Processing Subsystem
  - Myrinet crossbar (10)
  - Wafer Scale Signal Processor Segment (WPSG) No. 1 (11)
  - WPSG No. 2 (12)
  - Wafer Scale Signal Processor Management Processor (WMGT) (13)
- System/miscellaneous
  - Front (1) and back (16) connector segments
  - Power management layer A (9) for MSP subsystems and servo/guidance interface
  - Power management layer B (13) for Wafer Scale Signal Processor (WSSP) subsystems
  - Servo layer, which contains interfaces to communicate with servos, guidance (15)
  - Spare segment (8)

These 16 segments, referred to collectively as the Sensor and Fusion Engine (SAFE), have a common substrate size and I/O pad location. The physical size for substrates used in the DITP version of HIPP is 2 × 2 in., and up to 1000 I/Os can be accommodated on the surface of each segment.

8.4.2.1.2 Segment Layers

The contents of each segment can be completely different, and in fact the type of MCM technology used in each segment can be different so long as the segment definition is not violated. As such, layers do not necessarily need to be based on MCMs, but in fact could be single-chip packages, small PWBs, hybrids, or MCMs. In the terminology of HIPP, segments are said to contain one or more layers. Examples of possible layer arrangements within segments are shown in Fig. 8.48. Figure 8.48(a) illustrates a single-layer segment containing a single component mounted on a PWB. Figure 8.48(b) illustrates a single-layer segment containing one MCM. Figure 8.48(c) is an example of a segment with multiple layers, in this case two high-density interconnect MCMs. In principle, extremely dense MCMs could be used in multilayer arrangements, as shown here, to increase the volumetric densities of individual segments over that possible with a single-layer segment. Finally, Fig. 8.48(d) shows a single-layer segment in which a number of densely stacked 3D-chip configurations have been placed. In this manner, the HIPP packaging technology is versatile in that it can accommodate many existing modern forms of
single-chip, multichip, and 3D packaging.

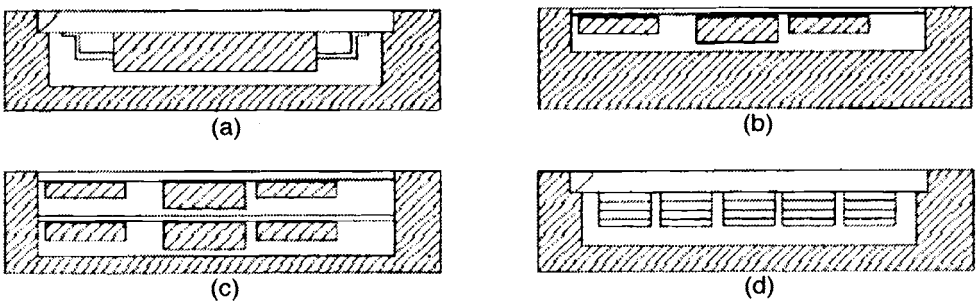

Fig. 8.48. Generic segment examples.

8.4.2.1.3 The Microbackplane and Assembly

As such, HIPP defines an efficient heterogeneous MCM-containment system. The deliberate stacking of segments is referred to as an assembly. Figure 8.47(a) gives a simplified, exploded picture of a HIPP assembly for clarity; Fig. 8.47(b) illustrates some of the special structures needed to integrate multiple segments into a complete assembly. These structures include the microbackplane, a number of interposers, an applique superstructure option for attaching more connectors or electronics, and hardware for secure segments to the microbackplane.

While each of the structures in Fig. 8.47(b) is essential, it is the microbackplane that uniquely defines the pattern of all interconnections in the DITP SAFE system (Fig. 8.49). The microbackplane is a compound flex system, based on a long manifold of multilayer copper-polyimide with orthogonal tabs of flex that address the face of every segment in the HIPP system. The microbackplane can be thought of as the "nervous system" of a HIPP assembly, and the design approach used for it combines the best elements of the two original HIPP concept designs shown in Fig. 8.46. Figure 8.47(b) illustrates the notion of clamshell mounting, a technique by which particular segments are mounted face-to-face through the microbackplane. Clamshell mounting allows a more intimate interconnection between two particular segments, which can serve to reduce complexity in the microbackplane.

Interposers form a springlike, compliant contact system, which mates the pinless conducting surfaces of segments to the tabs in the microbackplane. Such compliant inserts, which replace

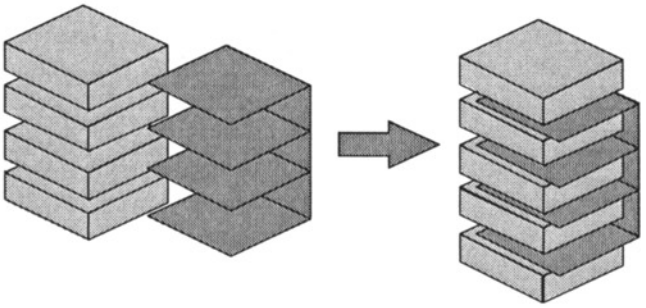

Fig. 8.49. Segment combination with microbackplane.

pins on ordinary packages, are necessary to ensure electrical continuity, exist between a large number of patterned conductors on flat surfaces. As shown in Fig. 8.50, an interposer is a compressible material that provides a conductive feedthrough, matching identical patterns on opposing surfaces. When the opposing surfaces are brought together, the interposer is compressed, forming electrical contact between the opposing surfaces. The compliance picks up any slack in irregularities between the otherwise flat surfaces to ensure a good contact. Since HIPP segments may contain up to 1000 I/Os, then so must the interposers. Since the pressure required to achieve the desired compliant travel range can be as high as 2 oz per contact, a significant amount of force could be required to tension the 16,000 total contacts possible in a DITP system. A "divide-and-conquer" approach is employed in the HIPP concept, involving localized tension of a smaller number of layers (usually one or two) to reduce the compressive requirements in the entire assembly. The concepts of segments, interposers, microbackplanes, and localized tensioning are illustrated in experimental assemblies shown in Fig. 8.51.

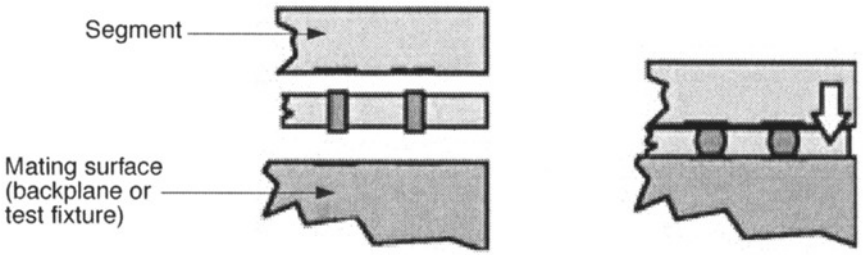

Fig. 8.50. Interposer detail.

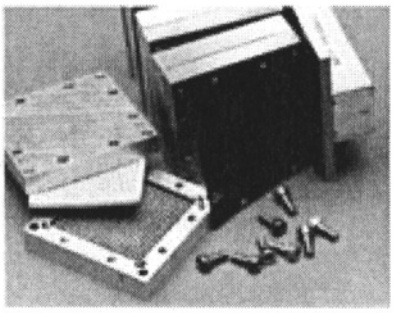

Fig. 8.51. Experimental HIPP assembly, exposing some segment details.

8.4.2.1.4 Power, Thermal, and Electrical Management

As a heterogeneous packaging system, the HIPP approach must deal with extremes in power management, thermal management, and signal integrity. Power delivery concepts under definition for HIPP are addressing the problem of delivery of 70–80 A of current at 3.3 V. Power delivery to systems with a large switched-signal content is a significant energy supply challenge. Also, the delivery of large amounts of current could require heavier metal structures than those available in a microbackplane. By contrast, only small amounts of current are required for analog sensors, but these current paths must have extremely low noise.

The thermal management in HIPP is hierarchical, based on first shuttling heat generated within each segment efficiently as possible to the outer edges of the segment walls and then coupling a second-level thermal management system. In the SAFE system, segment power dissipations range from about 1.5 W to 60 W per segment. Thermal transport in HIPP must occur laterally, parallel to the plane of the layers within the segments. This is because many HIPP assemblies are many-layer MCM assemblies, in which lateral transport is most important. Figure 8.52 illustrates the segment level thermal path. Segment thickness, segment wall thickness, and segment material selection can be based on local and global HIPP assembly needs. The second level of thermal management is application dependent, but must deal with power dissipation levels as high as 500 W for 16 segments. In the DITP SAFE assembly, as suggested in Fig. 8.52, lateral heat transport from segments into a phase change material is a second-level thermal management approach under consideration. For operation at longer intervals, a number of other options can be considered, ranging from heat sinks to heat pipes and liquid flow-through systems. Thermal management systems can more intimately link into segment walls, through texturing, flocking, insertion of flow-through channels, and other methods.

8.4.2.1.5 A New Packaging Hierarchy and Extensions of the HIPP Framework

HIPP establishes an alternate packaging hierarchy, one that is compatible with the existing hierarchy, but potentially much more efficient. L1 in the HIPP packaging hierarchy refers to internal layer composition, L2 is defined by layers within segments, L3 is defined by the segment itself, and L4 is defined as the HIPP assembly (of segments). Various forms of compatibility with the existing packaging hierarchy are readily achieved. For example, HIPP segments can be face-mounted onto PWBs through proper socketing or through conversion of the land grid array on the segment face to a ball grid array. Alternately, entire HIPP assemblies can be mounted onto a PWB, given the proper structural design. HIPP assemblies can be used to replace entire boxes; miniature connectors can be introduced on the front and back surfaces and onto the microbackplane itself.

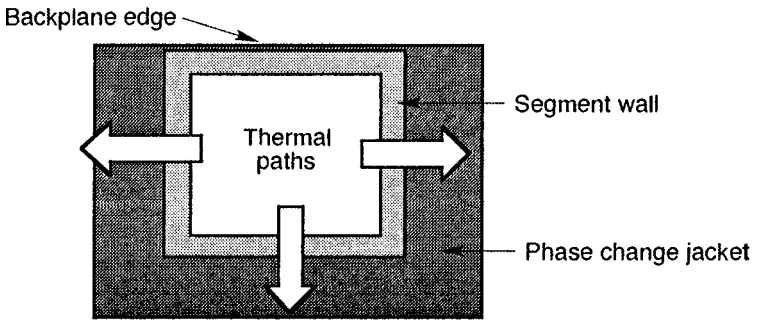

Fig. 8.52. Segment level thermal management.

HIPP offers a packaging system that meets the essential requirements of a 3D modular packaging system with high efficiency and flexibility. Segments are in essence interchangeable, reparable, and replaceable without great difficulty. In contrast to many 3D packaging approaches, HIPP can intermingle a great diversity of functional domains in electronics, providing in this way a great flexibility for system designers. Design guidelines under development will in time reduce to practice many aspects of the analysis needed to effectively use HIPP technology, such as electrical and thermal design rules and guidelines for exploiting CAD tools. It is believed that with these guidelines it will be possible to design HIPP-based systems with the ease and confidence one would use to design present-day VME or SEM-E (Appendix E of the military standard for standard electronic modules) board-based systems.

The HIPP-inspired packaging hierarchy may be further extended to include two additional levels: the cluster of assemblies (L5) and the cluster-stack (L6). Many potential concepts can be introduced to combine a number of HIPP assemblies into an efficient configuration that provides extremely high interassembly bandwidth and preserves good access of segment structures for thermal management. One such arrangement is shown in Fig. 8.53. Here, the cluster formation consists of a 2×2 arrangement of 16-segment assemblies [Fig. 8.53(a)]. A compound microbackplane [Fig. 8.53(b)] exploits short interassembly distances and affords a much higher interassembly bandwidth than nearly any other connector-based system, including present-day fiber optics. If the front and back of each assembly were fully exploited for I/O, the current HIPP standard would permit a signal transport of 8000 I/Os from the cluster. Two lateral edges of each assembly are available for thermal management, and the cluster could be completely encircled if necessary by an annular thermal management system. Figure 8.53(c) depicts a notional thermal management concept based on heat sinks.

Clusters of the nature described could be readily extended to form even more complex assemblies based on stacking clusters vertically to form cluster-stacks. The intercluster contacts could be accomplished with interposers, and system I/O and power delivery would be achieved through a connector system introduced at the top or bottom of the system. Such a stacked system has virtually no waste real estate; every part of the surface can be allocated to either thermal support or electrical transport (power and signal). In principle, the four-tier cluster-stack shown in Fig. 8.54 could aggregate well over one teraflop of processing within an approximately $5 \times 5 \times 4$ in. volume (exclusive of thermal management structures such as the heat sinks shown). This assertion is based on clusters of 16-segment assemblies, where each segment contains four layers of WSSP-based processing elements (each layer containing four WSSP components).

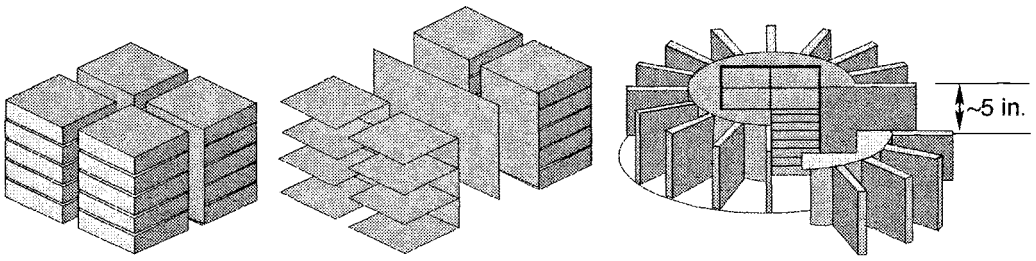

Fig. 8.53. Cluster arrangement of assemblies (extensions beyond present DITP embodiment).

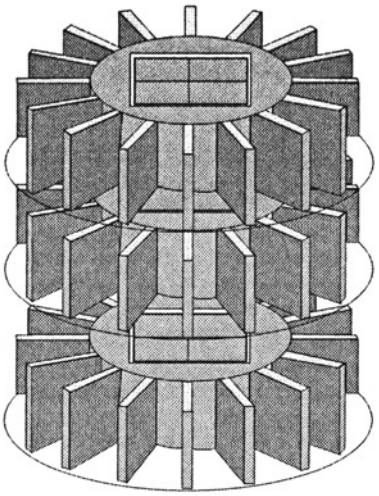

Fig. 8.54. Cluster-stack (teraflop concept).

8.4.2.1.6 Extensions of HIPP Through Improved Densities at L1

Beyond the extensions proposed for HIPP clusters and cluster-stacks, which provide a scheme for aggregating assemblies, the HIPP system can take full advantage of any new advances in microelectronics, MCMs, and 3D packaging technologies. HIPP can also take advantage of advances in connector, BGA, chip-scale packaging, and related technologies to increase segment I/O and system I/O densities. HIPP is then a framework for packaging, and new advances serve to accelerate further the density of this framework.

An example of such an accelerator is ultrahigh-density interconnect (UHDI). UHDI is centrally based around the idea of membrane-thin electronic MCMs. In the most aggressive form of this program, the electronic membranes are 0.002 in. thick, contain arbitrarily complex MCM circuits, and are flexible around structural contours or stackable into arbitrarily dense assemblies. The ideal UHDI system would use IC processes and designs optimized for this form of assembly, which could lead to significantly improved performance-to-power ratios (for example, 75% less power/MIP). In the simplest form, the first stepping-stone, existing ICs can be demonstrated functionally in substrateless versions of the HDI process (Fig. 8.55). Given that substrateless HDI is feasible, the remaining issues are solving crucial technical challenges in the four key UHDI research areas:

- Ultrathin semiconductor device processing
- Electronic membrane development and qualification
- 3D (membrane stacking) development
- Architectural optimization of 2D and 3D UHDI

Current AFRL-funding research is examining a number of these research areas. Recent experimentation on a limited scale has produced functional modules approximately 0.04 in. thick that contain four stacked substrates, compared with a normal single HDI module, which is normally 0.06 in. thick. This simple step alone quadruples the potential density of a HIPP segment based on HDI layer components. One potential application for the ultrathin UHDI technology is in congested MCM floor plans where planar arrangements of memory die can be replaced with compact tiles containing UHDI-based memory stacks. Such an approach can eliminate the space normally occupied by several components.

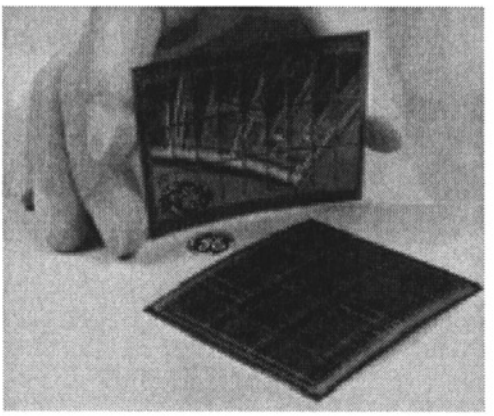

Fig. 8.55. Substrateless HDI technology.

8.4.3 A Third Generation of Advanced Packaging

If the ordinary hybrid microcircuits developed in the early days of space exploration can be considered a first generation of packaging, then surely the new emergent forms of MCMs in the late 1980s and early 1990s constitute a second generation. They differ not so much in role but rather in degree from their simpler precursors. While 3D approaches offer tremendous possibilities in extending the benefits of 2D MCMs in systems, they do not necessarily drive a change in the fundamental substrates. In fact, with approaches such as HIPP, first- and second-generation modules can be inserted with equal facility. Have we reached the end of improving the MCM, notwithstanding the obvious improvements gained, for example, by decreasing permittivity in the intermetal dielectric? Clearly not, given the trends in microcircuit technology. In fact, we believe it is possible to define a third generation of MCM technology, one that as before does not substantially differ in role but in degree. Coupled with the implied improvements in wiring density is the enablement of substantial improvements in 3D packaging by thinning. We introduce here the notion of hyperthinning in silicon, a domain in which silicon bends instead of breaking. The implications to conformal packaging, 3D systems, and integral passives are manifest. We believe the third generation of packaging will offer new challenges in design, both in complex homogeneous domains and mixed functional domains.

8.4.3.1 Density of Contacts and Wiring

Current MCM technologies are commonly limited to a 25–70-μm pitch. Technologies that can achieve a sub-10-μm pitch do so at the expense of performance, since in many such cases the dielectric and metal layers are thin, which gives rise to increased line resistance and capacitance. When the dielectric layers are not thin, then vias between two layers are often large to permit yieldable processes with good metal step coverages. What is needed in MCM approaches for the most advanced next-generation systems is a much greater line width for wiring density that has good electrical performance and permits high via and contact density. In this manner, both wiring and contact densities can be high enough to permit devices with many thousands of I/Os per cm^2 to be accommodated, consistent with the trends predicted by Rent's rule. The implications for patterned substrate designs are clear: only flip-chip approaches will suffice for high-density devices (devices that would force a perimeter wiring density below 35 to 40 μm). Such requirements are already met by advanced cryogenic hybrid detectors in which over 1 million contacts are made between a detector substrate (e.g., HgCdTe material) and a silicon readout IC at sub-40 μm using indium bumps.

It is important to note one impact of increased modular I/Os on the next level packaging systems, whether a 3D arrangement of MCMs or a tiling format onto boards. Precision alignment will be required at the next level of packaging. The alignment of modules at high density can be realized in two ways, using precision assembly approaches or using autonomous postassembly alignment, which we shall refer to as a two-phase connection approach. The former approach is tractable but highly undesirable for systems that would be fielded since servicing assemblies would require extremely specialized equipment (e.g., microscopes and micromanipulation/assembly equipment). In the case of a two-phase connector (shown in Fig. 8.56) an automatic alignment system affects a precision connection of two surfaces. The two-phase approach works by engaging coarse connection points under normal press fit connection tolerance (tens of mils). Then, after the first stage of connection, an active alignment system is activated that corrects for translation and angular misalignment. The precision sections of the assembly are then finally "docked." Such a two-phase concept could enable many thousands of I/Os between two surfaces to be efficiently interconnected.

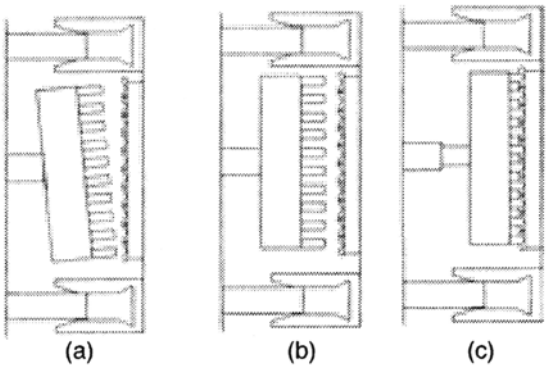

Fig. 8.56. Two-phase alignment sequence. (a) gross or coarse alignment after passive connection, (b) corrections made by active alignment system, (c) final connection made.

8.4.3.2 Hyperthinning and Its Implications

Typically semiconductor wafers are about 500 μm thick. For some packages, millions of devices are thinned in production to 0.007 in. In some 3D packaging approaches where thinning has occurred to 25–100 μm, silicon is observed to be very fragile and difficult to handle and process. At thinner extremes (< 25 μm), however, silicon becomes pliable (as shown in Fig. 8.57), completely changing the mechanical support/rigidity issues. This regime is referred to as hyperthin and creates a range of new possibilities in packaging.

The first obvious benefit is component density, particularly when patterned overlay technologies are used. With patterned substrate technologies, the height of the chip-attachment system (e.g., wire-bond loop height) will fundamentally limit density. In patterned overlay systems, the limiting factor is the height of the interconnect film, which is defined to be consistent with performance requirements. In other words, a 25–125 μm thickness in the patterned overlay sets the only limitation in how thin a hyperthin silicon MCM could be made. Layers this thin could be treated as electronic membranes, stacked like pieces of paper. If the layers could be permanently stacked, then it could be possible to laminate entire substrates together, forming connections in a manner analogous to interconnects between layers of the same MCM. Theoretically, especially for a system with low interconnect "intensity," such as a memory system, it is possible to form a

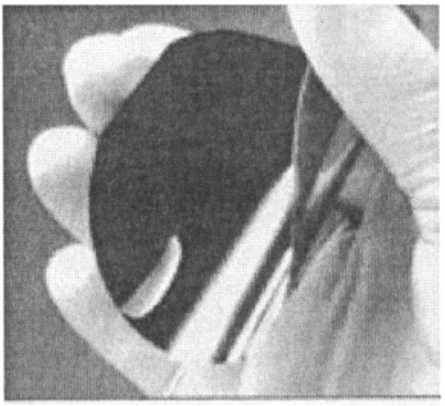

Fig. 8.57. Ultrathin silicon for specialty applications. (Courtesy Virginia Semiconductor.)

stack containing 500 MCMs/in., leading to a staggering 200 Gbits/cubic in. density based on 64 mbits/cm^2 in silicon memory technology

A second benefit of hyperthin silicon and overlay packaging is conformability, that is, the ability to bend substrates as though the flexible circuitry contained no components at all. As such, electronics could be formed like membranes and merged into structures of interest, planar and nonplanar, in ways never possible before. Computers could be wrapped around heat sinks, and distributed health monitoring systems "woven" into structures. The conformability raises interesting questions about the robustness of the packaging system. Does the silicon change its properties when bent? It has been shown that some insulators under pressure can become semiconducting, for example.[120]

A third speculated benefit of hyperthin silicon is improved radiation resistance. Since silicon substrates trap charge, which causes some radiation effects, by removing the substrate, radiation performance might be improved, which is a fundamental reason why silicon-on-insulator processes are of keen interest in radiation-hardened semiconductor research.

To be sure, the hyperthin silicon (or semiconductors in general) face significant challenges. In the case of dielectrically isolated silicon, a natural release layer may exist, permitting selective processing to remove the back of the die. Since most of the devices are built in bulk silicon, however, the hyperthinned approach is of little appeal unless a general thinning procedure can be found. Second, handling is a concern. If devices are thinned and then transferred to assemblies, the possibility of damage is great, and such an approach is likely to be very costly. One hope is that in using patterned overlay approaches, the die could be thinned *en masse* after they are bonded to the interconnection system. For HDI in particular, the ability to create substrateless MCMs (Fig. 8.55) could be particularly convenient in developing a system for creating hyperthin components without extensive special handling of individual components. Another concern in creating hyperthin MCMs is creating a compatible process for introducing capacitors and resistors. Some of the integral passive research may provide a solution, since discrete components do not necessarily lend themselves to thinning without destroying the components or their salient properties.

8.4.3.3 Next-Generation Design Approaches

The third generation of MCMs would place an increasing burden on the CAD infrastructure. Greater densities of interconnects and commingling of MCM and chip interconnect can create much more complicated design trade spaces. Exploiting fully the ultrathin systems when stacked

may promote specialty architectures, such as those explored in 3D monolithic wafer-scale integration.[121] In this approach, many parallel computers were partitioned into several subsections, each implemented on a different layer. Complete computers were formed only when all layers were stacked and interconnected. Finally, the ability to commingle functional domains remains a greater potential challenge in third-generation systems, given the significantly more complex signal integrity environment.

8.4.4 Advanced Multifunctional Structures

A sensible extension of packaging involves treating the structure of a system itself as part of the packaging solution. MFS refers to the general idea that structural members can serve other functions besides providing support. For example, a structure could be extended to serve the role of thermal management, signal and power distribution and/or generation, fluidic, and fiber-optic routing. While some examples of MFS can be found in ordinary life, no standard discipline exists for engineering MFS into systems.

Endowing structures with nontraditional functions is not an easy task. It is desirable to create a concept for MFS that promotes generality rather than inhibits it. Such generality promotes widespread use, which in time could lower cost through the economies of scale.

If MFS panels are to become the "LEGO™" blocks of future systems, then it is necessary to establish principles that permit a usable variation across a class of solutions for the things that MFS would functionally eliminate. For example, if an MFS panel were to replace power and signal distribution cables and harnesses, it would be necessary to either standardize the arrangement of signals on all panels, introduce concepts that allow changes to occur easily (e.g., reconfigurable interconnects), or both. The promise of MFS is realized when the technology can be shown to enable more rapid assembly of panels and more rapid configuration/reconfiguration of flight bus and payload systems. These benefits complement the potentially substantial reductions in size, weight, and power that could accrue when functions are handled by one set of structures as opposed to several.

What possibilities then exist for an MFS? A partial listing includes:

- Electrical power generation (embedded batteries and solar panels)
- Electrical power distribution (through high-power adaptations of flexible circuit technology)
- Electrical signal distribution (through multilayer flexible circuit technology)
- Microwave signal distribution (through low-loss, impedance control transmission line structures)
- Antennas (through surface-emitting dipole, microstrip patch antennas)
- Optical signal distribution (through embedded fiber-optic conduits/polymeric waveguides)
- Thermal management (through controllable heatpipelike structures within the MFS panel)
- Fluidic distribution (through standard distribution of embedded channels)
- Vibration control (embedded and distribution sensor, actuator, and control system)
- Distributed health and status monitoring (arrays of sensors in standard locations of each panel with built-in controllers and nonvolatile memory)

In each case, some concept of standardization and/or reconfiguration of channels is implied. Furthermore, in each case, a concept of socketing is implied. For effectiveness, socketing should be repeatable as necessary to permit rapid disassembly/reassembly.

8.4.4.1 Types of Electronics in MFS Systems

A possible organization of electronics subsystems in MFS-based spacecraft would divide the platform into bus-electronics and payload-electronics systems. Such a concept is illustrated in Fig. 8.58. In this approach, the bus electronics would be as invisible as possible, seemingly woven into

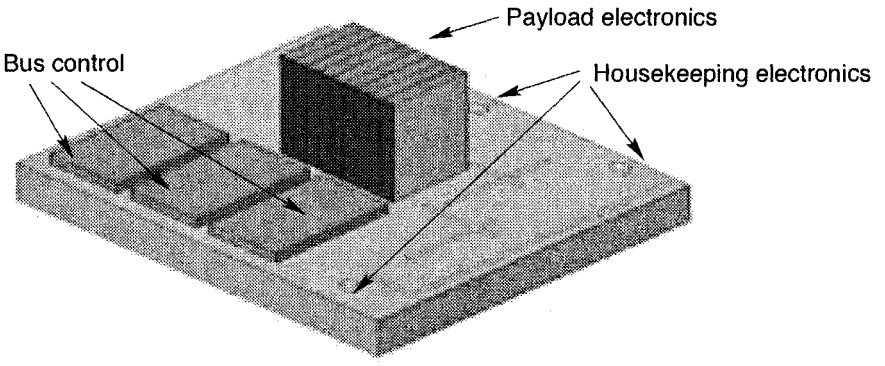

Fig. 8.58. Conceptual multifunctional structure panel.

the structure and putting little restriction on the placement of other functions. The bus electronics are broken into bus control electronics and distributed housekeeping electronics. The bus control electronics would deal with standard satellite control electronics such as a host processor, satellite communications, attitude control. The distributed housekeeping electronics, represented in Fig. 8.58 by a small low-power processor such as an AIC, would perform panel-specific sensor monitoring (e.g., pressure, temperature, dosimetry) and configuration management. It is envisioned that several AICs housed on each panel would perform these functions, working in concert with other panels as a self-organizing network, robust and tolerant of temporary or permanent failures of one or more nodes. The distributed housekeeping network would itself link to the spacecraft host processor through MFS interconnects within the panel.

Payload electronics are application-specific and introduced at specific docking points within the panel (shown in the center of Fig. 8.58). Here advanced packaging concepts such as HIPP can be used to implement, for example, a high-performance computation system or an integrated sensor payload. Specific mounting concepts must be developed to take full advantage of both the HIPP and MFS technologies, and intriguing possibilities exist, summarized in Fig. 8.59. For example, rather than employing a standard bolting arrangement [Fig. 8.59(a)], as one might do for a larger electronics box, it might be possible to employ a click-in-place system [Fig 8.59(c)] for a simpler attachment procedure to the MFS panel. The latter concept is particularly intriguing, as it allows for the possibility of in-situ placement/replacement of payload electronic assemblies. If the payload mounting areas are external to an MFS spacecraft, then the payload electronics can be serviced in orbit, without human intervention, creating the basis for a concept.

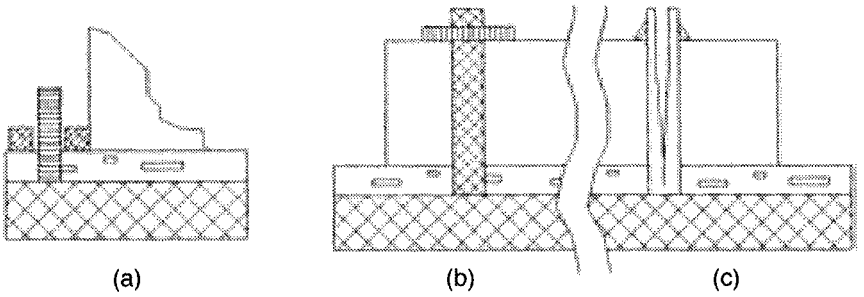

Fig. 8.59. Mounting systems. (a) bolt and bracket, (b) plate and cotter pin, (c) click-in-place assembly can be performed in flight.

8.4.4.1.1 Space Logistics Involving MFS and HIPP Technologies.

An overall, "hot-pluggable" electronics integration concept for in-orbit replacement of electronics on MFS panels is depicted in Fig. 8.60. Groups of layers or segments containing MCMs are combined with the necessary microbackplanes, shields, and protective layers to form an integrated HIPP assembly [Fig. 8.60(a–d)]. To effect a more intimate thermal management system, orthogonal fins protruding from the spacecraft panel could serve the dual purpose of improving thermal transport as well as providing a mechanical locking mechanism, similar to that shown in Fig. 8.60(c). The HIPP assembly is then integrated onto the spacecraft on the ground or in orbit [Fig. 8.60(e–f)]. To effect such a space logistics concept, improvements in connector technologies will be needed. Adaptation of existing interposer concepts could create an approach that automatically connects the payload to the spacecraft as the docking procedure is completed [Fig. 8.60(f)].

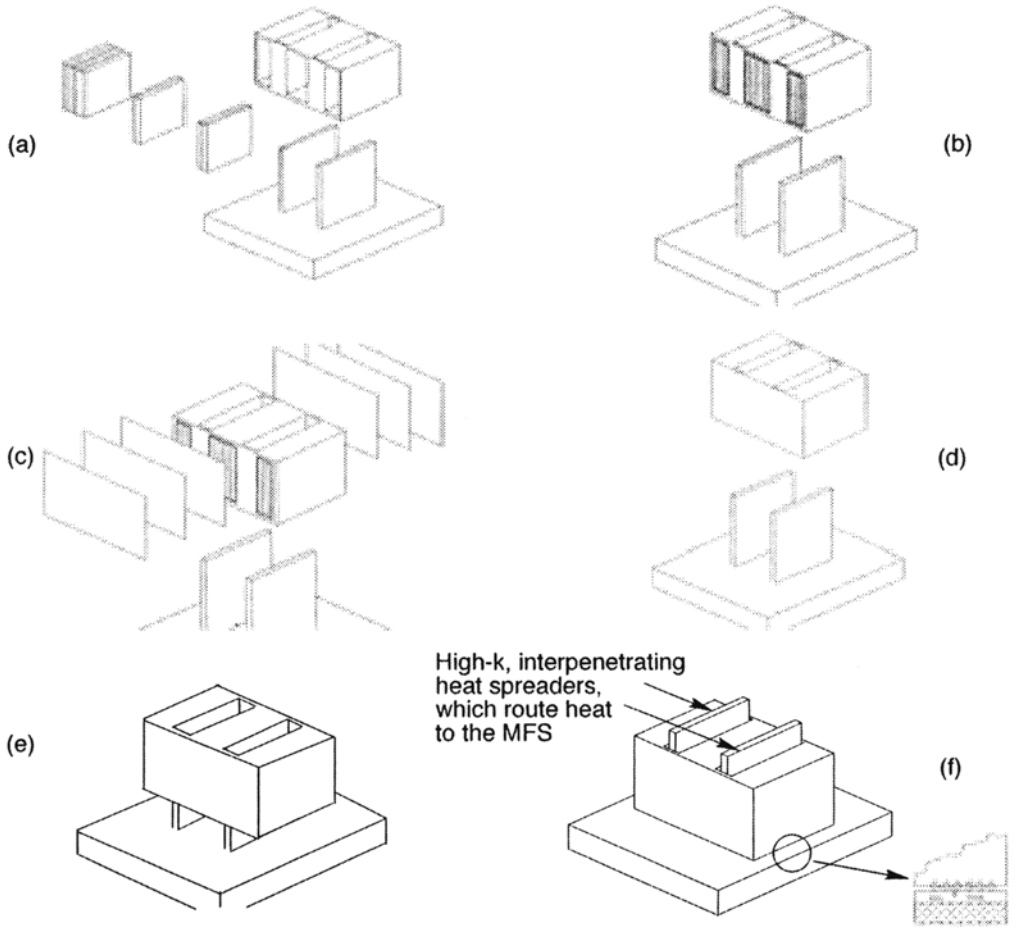

Fig. 8.60. MFS in-orbit "hot-plug" concept for space logistics. (a) HIPP assembly, exploded view, before integration; (b) HIPP assembly with integrated electronics; (c) addition of microbackplane, shielding, and protective layers; (d) a completed HIPP assembly, representing payload electronics for example, ready for integration onto panel; (e) partially integrated assembly; (f) fully integrated assembly, showing detail of underside flush-mount interposer system that electrically connects payload to MFS interconnection manifold formed on panel surface.

8.4.4.2 MFS Interconnection Manifolds

For purposes of affordability, the need to standardize MFS interconnection structures is manifest. Yet as previously discussed, the desired properties of interconnections are domain-specific. Hence, it is not possible to establish a "one size fits all" signal and power distribution scheme. As such, some regions of the MFS interconnection manifold might be optimized for power, some for digital, and still others for microwave and for analog.

8.4.4.2.1 Power Interconnection and Distribution within an MFS Panel

Power interconnections, which require low-resistance and sometimes high-current conductors, could be routed along gridlines, with branches from the grid to service particular points on the MFS panel corresponding to areas where bus electronics would be attached, mounting points for payloads. Figure 8.61 depicts a simplified grid. The metallization for the power grid would be robust enough for high-amperage power distribution, much heavier than needed for any other signal type. On some panels, where no special high-power electronics are mounted, the grid would simply "pass through" power to another panel. Each of the power "bars" would in fact be a collection of power conductors that can be separated for multiple voltage connections. Unused conductors on the power bars could be shorted together for lower loss power delivery. Discrete and specific regions of each panel could serve as tapping points for the various power lines passing through a panel. These regions, referred to as power service points (PSP), provide convenient supply points for electronics introduced *post facto*.

Power routing of the interconnections could be accomplished with three distinct methods. The first method, *a priori* routing, is reserved for the bus electronics, which are to be an intrinsic part of the panel. This type of power conductor routing could represent a deviation from the standard grid scheme, especially for distributed health and status monitoring networks, which are typically fairly low-power functions needed for less robust interconnection. The other two power routing methods rely on a number of power switch routing nodes (PSRN). PSRNs, in this concept, contain a number of links that allow "horizontal" power conductors to electrically connect to either "vertical" conductors (to map a voltage source to a load) or to another horizontal conductor (to increase current-handling capability of a particular voltage). In the second routing method, integration-point routing, the interconnecting links in PSRNs are "hard-wired," that is, prefabricated and

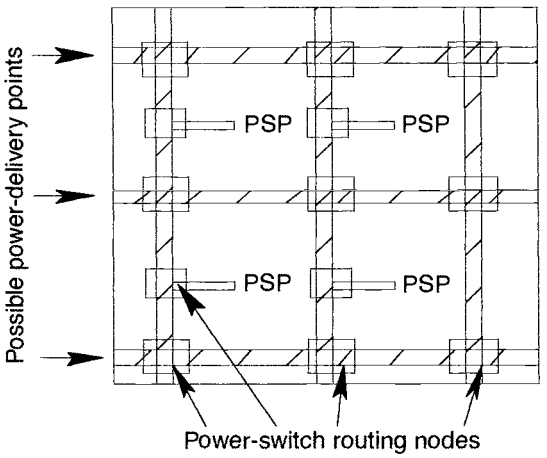

Fig. 8.61. Conceptual power routing manifold for an MFS panel.

installed during spacecraft integration. While this method preserves flexibility of MFS power routing until fabrication, it does not permit any flexibility after integration is completed.

This limitation is overcome by the third method, run-time routing, in which link connections are programmable within the panel and are reconfigurable even after integration and theoretically after launch. Configuration information on links for a panel can be stored in nonvolatile form within housekeeping electronics resident in the panel. At worst, the link elements that would be required would have to be nonvolatile and bistable themselves, and would necessarily have to preclude the possibility of glitching during spacecraft operation. The most significant barrier in the run-time routing concept, which enables plug-and-play spacecraft, is finding a bistable link-formation mechanism. Solid-state switches cannot be employed for the mechanism because such switches need to be at a particular threshold voltage with respect to power rails. As the rails are dynamic, it is impossible to guarantee that all switches can maintain the proper electrical relationship. Furthermore, power switches are subject to radiation effects, which can serve to increase on resistance. One technology not subject to this limitation is MEMS-based relays. In AFRL research, concepts for bistable MEMS relays (Fig. 8.62) suitable for such applications have been defined for inclusion in monolithic arrays and even within interconnections of an MCM. The number of such relays required is $(n^2-n)/2$ for nonblocking permutations of n different conductors, which is beyond reach of any non-MEMS relay technology. Fortunately, with MEMS-based switch approaches, it is possible to place a very high density of these switches within the space required of a PSRN.

Given the trends for continuing decreases in voltage for microelectronics, other issues remain for power distribution within a spacecraft, which makes the effects of I^2R losses caused by conductor resistance increasingly pronounced. Localized (point-of-load) power distribution will be realistically required at or below 3.3 V, even in small spacecraft. As such, some consideration is required for inclusion of such power converters directly within the MFS panels. Currently such converters are selected based on somewhat rigid specifications of input voltage, output voltage, and load conditions. With breaking improvements in radiation-hardened electronics, MEMS switches, integrated magnetics, and power-converter topologies, "smart power" is possible. Such smart-power converters could be reconfigured in-system, perhaps dynamically, to adjust for variations in voltage and load, considerably improve robustness and conversion efficiency.

In considering the issue of power distribution, it may make sense to also consider power generation/storage within the panel. In traditional spacecraft, power-combining electronics operate centrally and distribute power throughout the spacecraft. Other schemes based on a distributed power generation scheme should also be possible, eliminating a large amount of electronics devoted to centralized power management. The advent of the thin-film battery and solar-power technology might make possible the creation of panels that literally "carry their own weight" with respect to power generation, storage, distribution, and dissipation.

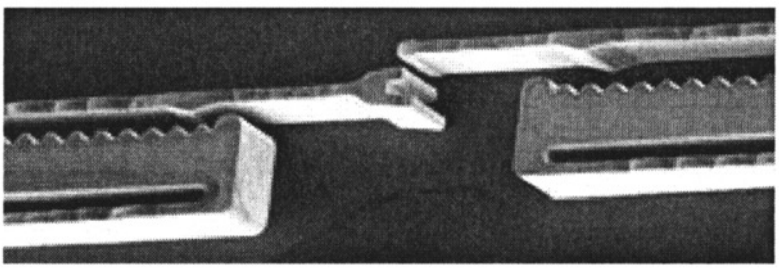

Fig. 8.62. LIGA-based bistable relay (courtesy Maj. John Comtois, AFRL).

8.4.4.2.2 Digital Interconnections within an MFS Panel

Digital connections within an MFS panel correspond to digital discretes, busses, and other general-purpose wiring. The digital interconnections are more tolerant of series loss and isolation in comparison to power interconnections, but unfortunately occur at a much higher density. It is envisioned that many hundreds of I/Os could be required for an average panel. As such, it is necessary to consider large groups of wires routed as in Fig. 8.61. In some cases, this can be done "virtually," that is, with FPGA or field-programmable interconnect devices. This approach assumes relatively low-signal frequency content, which is not true for many high-speed bus structures. When the interconnection distance exceeds a lumped element distance, transmission lines exist in the interconnect, requiring proper terminations. This situation is compounded considerably by the many naturally occurring discontinuities in the interconnection manifold. Once again, the use of MEMS switching devices could combat this complexity by effectively eliminating some of the transmission line stubs that would otherwise exist in the interconnection manifold.

8.4.4.2.3 Analog Interconnections within an MFS Panel

Analog signal types are classified as: low-frequency instrument (<1 MHz), high-frequency instrument (>20 MHz), and power analog. Interconnections that bear instrument-class analog signals have strict signal integrity requirements, chiefly in series attenuation and isolation from crosstalk. It is possible to form sophisticated shielded quasi-coax interconnections. And the quantity of such interconnections is higher than that required for power delivery, but not as high as for the complex digital portions of typical systems circuitry. Distributed, embedded analog signal capture nodes, which can be formed with a network of AICs laminated into the panel structure, greatly simplify the management of many dozens or hundreds of signal monitoring points. Such a network would localize AICs physically near the points where analog signals are generated, alleviating the need to protect long-distance analog signals from loss and crosstalk. Higher-performance analog measurement needs can be accommodated through higher-performance capture modules similar to AICs but with higher bandwidth. Here, transmission line effects could be problematic. Finally, power analog signals, associated with motor drive, require significantly larger conductor cross sections to minimize power delivery loss.

8.4.4.2.4 Microwave Interconnections within an MFS Panel

Microwave interconnections pose one of the greatest challenges in an MFS system, as microwave signals are subject to most of the previous concerns in signal integrity except for high wiring density. Impedance control for a fixed interconnect arrangement is difficult without the desired adaptive properties needed for a plug-and-play spacecraft. Finding switch configurations with low-loss and high bandwidth is not trivial, nor is designing the associated transition configurations to appropriate interconnection manifolds. Here, interconnections can generically be established in several arrangements for planar media (e.g., stripline, microstrip, coplanar waveguide, coplanar strip, and slotline). Figure 8.63 illustrates an evaluation approach for prospective MEMS switches that might operate at microwave frequencies.

If MEMS switches and flexible interconnection manifolds can be shown adequate for microwave applications, then some novel concepts might be exploited to more readily establish an adaptive system in which several interconnection paths could be formed for different applications using the same panel. It is possible, for example, that MEMS devices could create a tunable impedance manifold. Several concepts for this include the use of a transmission line in which a series of MEMS louvers adjust path impedances and implement MEMS-tunable stubs. The former concept, illustrated in Fig. 8.64, can tune the impedance of a transmission line with a dielectric of permittivity ε_1 by using small pieces of material attached to MEMS levels with higher

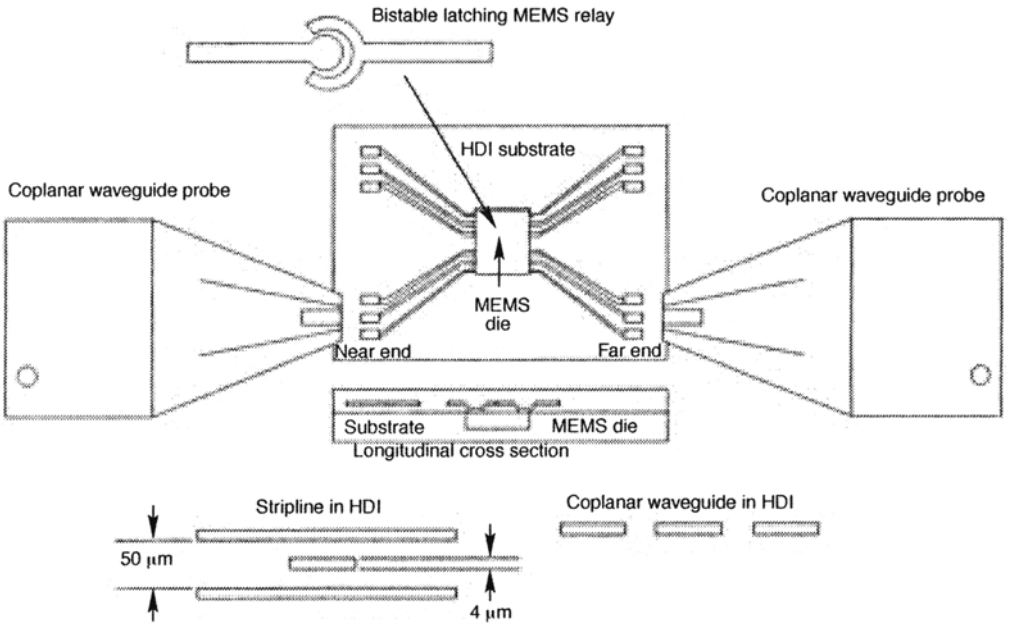

Fig. 8.63. MEMS switch test configuration.

permittivity (ε_2). Adjusting the positions of the MEMS louvers can alter the localized effective permittivity of the transmission line, permitting fine-scale impedance control. A second MEMS concept, that of tunable stubs, can employ relays similar to those shown in Fig. 8.61 to physically add or take away conductors and circuits, permitting some potentially useful adjustments in the microwave sections of a design.

8.4.4.3 Panel-to-Panel Attachment/Connection

The ability to attach multiple panels together and connect the various MFS features properly is an obvious requirement. Let us introduce the concept for a generic MFS "tile" of the right dimension to accommodate a wide range of possible satellite types and functions. The tile should have:

- Good structural characteristics
- Ability to form larger structures through tiling
- Ability to support assembly with more than one attachment angle to address vertices
- Ability to be stacked densely in a stowed configuration for mass deployment and in-space assembly

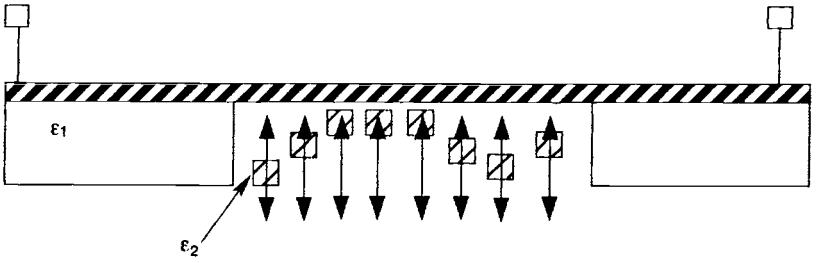

Fig. 8.64. MEMS-tunable transmission line.

A notional example of such an MFS tile is shown in Fig. 8.65. The particular geometry need not be hexagonal as chosen here, but should be chosen to permit flexibility in possible arrangements. The tile can be attached from any of the six edges shown; one mounting post or threaded insert is shown in the center. Larger planar arrangements are readily formed through juxtaposition as shown in Fig. 65(b), and payloads attached on a standard grid, as shown in Fig. 65(c).

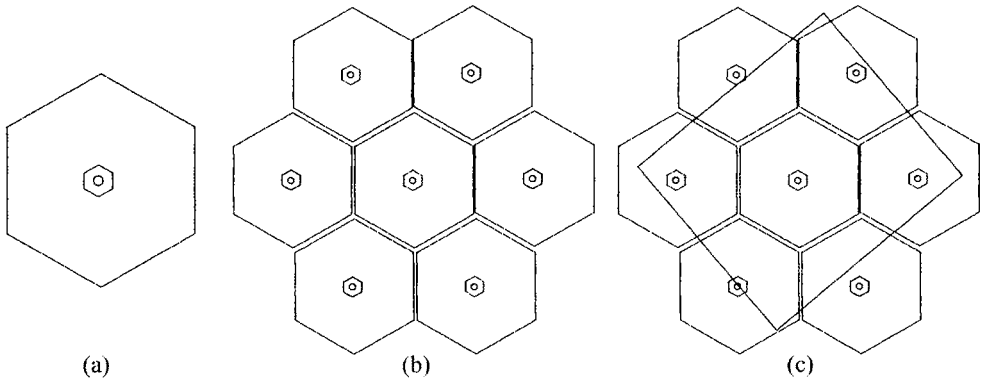

Fig. 8.65. MFS panel connections. (a) fundamental MFS tile, (b) tiles arranged to form larger planar structure with central payload attach point, (c) application of payload assembly that spans a number of the payload mounting points.

In this concept of panel-to-panel attachment, it would be important to support the ability to mount at certain angles to form boxlike and other polygonal shapes from which a system could be built. As shown crudely in Fig. 8.66, such a system would allow both planar and nonplanar engagement angles. Novel concepts for the joining process itself are suggested from other MEMS and non-MEMS sources. Large, coarse grids of panel-to-panel conductors correlate well with ordinary mechanical fitting tolerance and are readily accommodated by plug-and-socket arrangements. Dense conductor clusters, some optoelectronic and fluidic, and other connections will require greater precision in assembly, suggestive of a two-phase connection system as depicted in Fig. 8.57. The structural requirement for panel-to-panel attach will require good mechanical contact at several engagement angles. Perhaps this requirement can be addressed by special detented mechanisms involving shape memory actuation, which could be employed for the primary mechanical connection system. For ground assembly, more conventional techniques could be employed, but the big advantages are joining mechanisms in space for plug-and-play spacecraft.

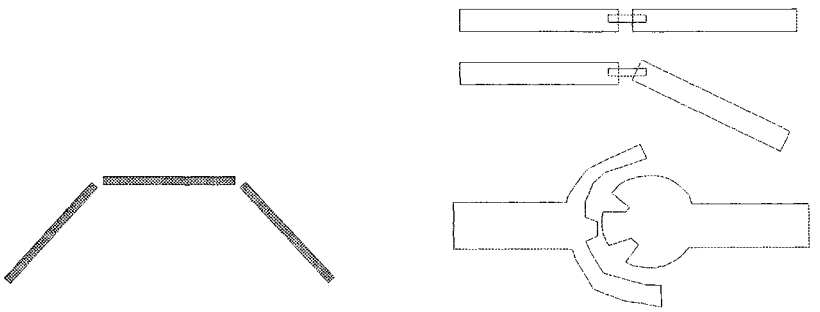

Fig. 8.66. Depiction of nonplanar engagement of panel and suggestion of detented attachment connection.

8.4.4.3.1 Extension to Space Logistics

If the several aforementioned elements of MFS design can be applied, then it is possible to consider satellites that can be serviced in orbit. Such a hypothetical repair operation is posed in Fig. 8.67. In this case, the faulty MFS panel [shown in Fig. 8.67(a) as a non-colored tile] is identified, and its edge connections are disengaged, permitting removal [Fig. 8.67(b)]. A known good tile is used for replacement and is inserted in the location previously occupied by the faulty tile [Fig. 8.67(c–d)]. Though a number of practical issues must be addressed to implement this space logistics concept, a number of powerful advantages clearly exist, such as spacecraft reuse (good tiles recovered from decommissioned spacecraft).

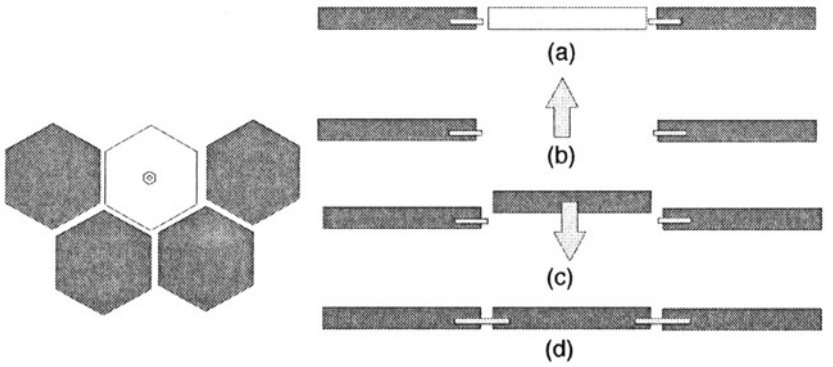

Fig. 8.67. Space logistics concept. Plan view (left), longitudinal view illustrating sequence (right). (a) Defective panel noncolored, (b) released from spacecraft, (c) new tile panel added, (d) completed replacement.

8.5 Conclusions

This chapter addresses the technologies of advanced electronics packaging. Packaging is primarily enabling to the extent that it allows the outside world to access functions contained within packages, recursively defined through a hierarchy that spans from the transistor to the system platform. Specific packaging concepts, especially those involving 2D and 3D MCMs, are discussed here as a practical introduction to the state of the art in electronics packaging. A review of the principles of package engineering includes discussion of the drivers for the materials and geometries of packages, substrates, and their respective configurations within systems, as well as the system design philosophy in which packaging is integrally considered. We present a number of advanced techniques and case studies in packaging and what we believe is an enabling heterogeneous 3D packaging concept, one that deliberately exploits the most promising microcircuit, MCM, and 3D packaging. This framework extends to the future of packaging—a "third generation" of packaging. Finally, in MFS, we consider both the challenge and the enabling benefits of approaches that can lead to LEGO™-like spacecraft, in which both ground and space assembly concepts are possible.

Packaging is the wrapper and mapper of systems at various levels. It is useful, in some respects, not for what it does but for what it does *not* do, such as *not* delaying or distorting signals, *not* restricting thermal transport, *not* contaminating sensors. By the same token, packaging is an enabler, as it enables a system to access the capabilities of disparate components. The goal of advanced packaging is to do this very well, even to the theoretical limits of what components can deliver.

8.6 References

1. M. J. Little and C. T. Moberly, *Signal Processing Systems Packaging-1*, Rome Laboratory Technical Report no. RL-TR-92-95 (April 1992).
2. R. Iscoff, "Wire Bonders—Stretched to the Max?" *Semiconductor Int.* **54** (2), 52–4, 56 (February 1993).
3. J. D'Ignazio, "Wirebonding's Reign Continues," *Semiconductor Int.* **19** (6), (June 1996).
4. R. Bidin, "High Pin Count Wirebonding: The Challenge for Packaging," *Solid State Technol.* **35** (5) 75–7 (May 1992).
5. Assembly Products, 97 East Brokaw Road, Suite 100, San Jose, California 95112-4209.
6. D. Maliniak, "MCMs Traverse the Cost Curve," *Electron. Design* **43** (13) (June 26, 1995).
7. J. Vardaman, president, TechSearch International, Austin, Texas (private communication, 1996).
8. "There's Magic in That Chip," *Electron. Products* (April 1995).
9. Harris Corp. literature on the Digital Drop Tuner (1995).
10. R. F. David, "Manufacturing Power Hybrid Circuits," *Electron. Packaging and Production* **36** (3) (March 1996).
11. "Module Provides Upgrade Path for Pentium Laptops," *Computer Design* (April 1997).
12. MicroModule Systems: http://www.mms.com/products/geminidoc/web_r20.htm.
13. nChip Corp., now Flextronics International Ltd., 2241 Lundy Ave., San Jose, CA 95131-1822.
14. *Microwave HDI Design Guide* (GE Corporate R&D Center, Schenectady, NY, 1995).
15. M. McNulty, *et al.*, "Microwave MCMs Using Low-Cost Microwave Chip-on-Flex Packaging Technology," *High Density Interconnect* **1** (1), May 1998.
16. *Chip on Flex High Density Interconnect Design Rules* (Revision 3) (GE Corporate R&D Center, Schenectady, NY, July 1997).
17. J. C. Lyke, "Two- and Three-dimensional High Performance, Patterned Overlay Multi-chip Module Technology," *Proceedings of NASA Technology 2002:Third National Technology Transfer Conference* Vol. 1 (December 1992), pp. 195–204.
18. J. D. Reed, *et al.*, "High Frequency IC to IC Signaling on Rapidly Prototyped Flip Chip MCM-D Substrate," *Proceedings of the International Conference and Exhibition on Multichip Modules and High Density Packaging* (Denver, 15 April 1998).
19. QTAI, MCC: http://www.mcc.com/projects/fmm/.
20. R. Iscoff, "Wafer Scale Integration: An Appraisal," *Semiconductor Int.* **7** (9), 62–65 (September 1984).
21. J. Banker, "Reducing Cycle Time Through Programmable Multichip Modules," http://www.pico-sys.com/red_cycl.htm.
22. "Advanced Packaging Gives SMT New Life," *Electron. Eng. Times* (6 September 1996).
23. S. Berry, "Reaching HDI Comfort Levels," *High Density Interconnect* **1** (1), 14–16 (1998)
24. "Component Packaging Technologies Enhance PCB Performance," *Electron. Packaging and Production* (January 1998).
25. A. Bindra, "TI Eyes New Package Type," *Electron. Eng. Times* (3 June 1996).
26. D. Strassberg, "More Pins and Less Space Beget New IC Packaging," *EDN* (25 May 1996).
27. "BGA Update," *SMT* (April 1998).
28. "Motorola Gate Arrays Span 12 K to 278 K Gates," *Electron. Eng. Times Product File.*
29. Y. H. Pao, *et al.*, "BGAs in Automotive Applications," *SMT* (January 1998).
30. P. Mescher, "The Evolution of BGA," *Advanced Packaging* (March 1996).
31. M. S. Cole and T. Caulfield, "Ball Grid Array Packaging," *EDN Products Edition* (15 August 1994).
32. T. LaMarche, "X Ray Closes the Inspection Loop," *Evaluation Eng.* (September 1993).
33. E. Williams and D. Duschl, "Effective Rework with Convective Tools," *SMT* (May 1998).
34. T. Costlow, "LSI Rolls Enhanced BGA," *Electron. Eng. Times* (6 March 1995).
35. "More BGA Choices Emerge," *Electron. Products* (April 1995).
36. J. Lipman, "New IC Packages Really Pack in the Leads," *EDN Europe* (1 September 1997).

37. R. DeJule, "High Pincount Packaging," *Semiconductor Int.* **20** (8), 139–140, 142, 144, 146 (July 1997).
38. R. A. Munroe, "Ball Grid Array Technology," *EDN Products Edition* (8 August 1997).
39. "Dimpled Ball Grid Arrays," *Semiconductor Int.* (June 1997). See also http://www.kyocera.com/kai/dbga.html.
40. R. D. Schueller, "Portable CSP," *Advanced Packaging* **7** (4), 28–30, 32, 34 (May 1998).
41. A. Seung-Ho and Y-S. Kwon, "Popcorn Phenomenon in a Ball Grid Array Package," *IEEE CPMT—B* **18** (3) (August 1995).
42. R. Ghaffarian, "BGAs for High Reliability Applications," *Electron. Packaging and Production* (March 1998).
43. G. Derman, "Socket Suppliers Target Emerging High-density World of Ball- and Land-grid Arrays," *Electron. Eng. Times* (January 1998).
44. R. Ghaffarian, "CSPs Assembly Reliability," *Advancing Microelectronics*, **24** (6) (November 1997).
45. T. DiStefano and J. Fjelstad, "Chip-scale Packaging Meets Future Design Needs," *Solid State Technol* (April 1996).
46. A. Bindra, "Flex Circuits Branch Out," *Electron. Eng. Times* (19 August 1996).
47. R. Ghaffarian, "Reliability of Chip Scale Packages," *EEE Links* **4** (1), (January 1998), publication of NASA/GSFC, http://arioch.gsfc.nasa.gov/32/Linkspg.html.
48. S. Greathouse, "Chip Scale Packaging Breaks New Frontiers," *Solid State Technol.* (March 1996).
49. J. Vardaman, "CSPs: Hot New Packages for Cool Portable Products," *Solid State Technol.* (October 1997).
50. N. Takahashi *et al.*, "Three-Dimensional Memory Module," *IEEE CPMT—B* **21** (1) (February 1998).
51. M. Donlin, "IC Packaging Moves to the Front of the Design Cycle," *Computer Design* (July 1994).
52. "Dense Memory Stacks Hold up in Space," *Military and Aerospace Electronics* (January 1997).
53. Cover, *Solid State Technol.* (October 1992).
54. Dense-Pac Microsystems, Inc., advertisement mailer (7321 Lincoln Way, Garden Grove, CA 92641-1428).
55. "Worldwide Connector Sales Continue to Grow," *Electron. Packaging and Production* **37** (9) (10 July 1997) and private communication with Ron Bishop of Bishop & Associates (July 1997).
56. R. R. Tummala and E. J. Pymaszewski, *Microelectronics Packaging Handbook* (Van Nostrand Reinhold, New York, 1989).
57. L. L. Moresco, "Electron. System Packaging: The Search for Manufacturing the Optimum in a Sea of Constraints," *IEEE Trans. Components, Hybrids, Manufacturing Technol.*, 13 (2), 494-508 (September 1990).
58. N. Weste and K. Eshraghian, Principles of CMOS VLSI Design (Addison-Wesley, New York, 1985).
59. M. A. Fury, "Emerging Developments in CMP for Semiconductor Planarization," *Solid State Technol.* (April 1995).
60. "A Look at the Worldwide IC Packaging Market," *Electron. Design* (24 June 1996).
61. H. B. Bagoklu, *Circuits, Interconnections, and Packaging for VLSI* (Addison-Wesley, New York, 1990).
62. J. Lyke and J. Tausch, "Development of a High Performance 800-pin Count Package for 3-D WSI Systems," *Proceedings of the 1992 Government Microcircuits Application Conference* (Las Vegas, Nevada, November 1992).
63. E. J. Pymazewski, private communication (1992). (See Ref. 55.)
64. "Effects of Interconnect Granularity," http://www.ai.mit.edu/projects/transit/rcgp/chapter1.6.1.html.
65. D. P. Seraphim *et al.*, *Principles of Electron. Packaging* (McGraw Hill, New York, 1989).
66. B. W. Kernighan and S. Lin, "An Efficient Heuristic Procedure for Partitioning Graphs," *Bell System Tech. J.* **49** (2), 291-308 (February 1970).
67. J. Lyke, "Efficient Heterogeneous Three-Dimensional Packaging at a System Level," *Proceedings of the 16th DASC Conference* (AIAA/IEEE) (Irvine, CA, 26–30 October 1997).

68. J. Butler *et al.*, "Adapting Multichip Module foundries for MEMS Packaging," *Proceedings International Conference and Exhibition on Multichip Modules and High Density Packaging—MCM '98* (Denver, Co, 15–17 April 1998), pp. 106–111.
69. R. S. Irwin, "Solder Self-Assembly for MEMS," *Proceedings of the 44th International Instrumentation Symposium* (Reno, NV, 3–7 May 1998).
70. P. Cook, "Silicon Micromachining Applied to the Management of the Thermal Environment in Wafer Scale Integration Technology," Master's thesis, Air Force Institute of Technology (1992).
71. P. Madden, "Microvias Take Center Stage," *Printed Circuit Design* **15** (2) 19–22 (February 1998).
72. V. Adams *et al.*, "Low Cost Packaging for Accelerometers," *Electron. Packaging and Production* (December 1993).
73. T. Sudo, "Present and Future Directions for Multichip Module Technologies," *IEEE J. Solid-State Circuits*, 30 (4), 436–441 (April 1995).
74. C. T. Gray *et al.*, *Wave Pipelining: Theory and CMOS Implementation* (Kluwer Academic Publishers, Boston, MA, 1994).
75. J. C. Lyke, "Silicon Hybrid Wafer Scale Integration Interconnect Evaluation," Master's thesis, Air Force Institute of Technology (December 1989).
76. G. Hutcheson, "Ten Trends Shaping the Next Ten Years," *Solid State Technol.* (May 1997).
77. R. E. Sigliano, *et al.*, "Multilayer Ceramics: a Revitalization," *Electron. Packaging and Production* (September 1996).
78. S. Chillara *et al.*, "Build-up Laminates Used in High Density Applications," *Electron. Packaging and Production* (August 1997).
79. G. L. Kmetz, "Designing Copper-Trace Resistors," *Electron. Design* (13 May 1996).
80. W. Ko and M. Pecht, "Humidity and Corrosion Analysis and Design," in *Handbook of Electronics Package Design*, edited by M. Pecht (Marcel Dekker, Inc., New York, 1991).
81. J. J. Licari and L. R. Enlow, *Hybrid Microcircuit Technology Handbook* (Noyes Publications, Park Ridge, New Jersey, 1988).
82. G. N. Ellison, "Thermal Analysis with Affordable Programs," *Proceeding of the 5th Annual International Electronics Packaging Conference* (1985).
83. S. Dakuginow *et al.*, "Thermal Measurement Standards for ASIC Packaging," *Semiconductor Int.* (June 1996).
84. C. P. Minning, "Thermal Management," in *Multichip Module Design, Fabrication, and Testing*, edited by J. Licari (McGraw-Hill, Inc., 1995).
85. B. Ozmat "Interconnect Technologies and the Thermal Performance of MCM," *IEEE Trans. Components, Hybrids, Manufacturing Technol.*, **15** (5), 860–869 (1992).
86. L. S. Fletcher, "A Review of Thermal Enhancement Techniques for Electron. Systems," *IEEE Trans. Components, Hybrids, and Manufacturing Technol.* **13** (4), 1012–1021 (December 1990).
87. D. B. Nor, "Mechanical Aspects of Multichip Module Reliability," *JOM* **44** (7), 29–35 (July 1992).
88. C. Libove, "Rectangular Flat-Pack Lids Under External Pressure," Rome Air Development Center Technical Report, RADC-TR-76-118 (May 1976).
89. J. H. Comtois, "Structures and Techniques for Implementing and Packaging Complex, Large Scale Microelectromechanical Systems Using Foundry Fabrication Processes," Ph.D. thesis (Air Force Institute of Technology, 1996).
90. R. E. Albano and J. P. Keska, "Is Design Realization a Process? A Case Study," *IEEE CHMT* **13** (3) (September 1990).
91. B. J. MacLennan, "Who Cares About Elegance?" University of Tennessee, Knoxville, Technical Report no. UT-CS-97-344.
92. J. D. Cho *et al.*, "High Performance MCM Routing," *IEEE Design and Test of Computers* **10** (4), 27–37 (December 1993).
93. Q. Yu *et al.*, "Algorithmic Aspects of Three-Dimensional MCM Routing," *Proceedings of 31st ACM/IEE Design Automation Conference* (San Diego, 6–10 June 1994).
94. D. Maliniak, "MCMs Traverse the Cost Curve," *Electron. Design* (26 June 1995).

95. Charles Stein, ARL/VSSE (private communication, October 1998).
96. N. Virmani, Nick and Kusum K. Sahu, "Reliability and Radiation Sensitivity of Plastic Encapsulated Microcircuits in space Applications," Report prepared for NASA Goddard Space Flight Center Report, Log no. EPG-007-93.
97. G. Rose *et al.*, "Fundamentals of Plastic Encapsulated Microcircuits for Space Applications," presentation by the NASA Parts Project Office (October 1994).
98. For example, http://misspiggy.gsfc.nasa.gov/og/ and http://msfcpec1.msfc.nasa.gov/eh12/outgas.html contain downloadable information.
99. A. Garrison "Case History—GGS Sensor Module Chip on Board Evaluation," NASA Goddard Space Flight Center Code 312 (1993).
100. D. Duston *et al.*, "COTS-grade Electronics Set to Escape Earthly Bounds," Military & Aerospace Electronics (December 1995).
101. M. Pecht, "Plastic Encapsulated Microcircuits: the Hardness Assurance Committee of the NASA/AFSMC Space Parts Working Group," briefing (Alexandria, VA, 20–22 May 1996).
102. S. Clark, *et al.*, "Plastic Packaging and Burn-in Effects on Ionizing Dose Response in CMOS Microcircuits," *Proceedings of IEEE Trans. On Nuclear Sci.* **42** (6) (December 1995).
103. C. P. Wong, "Understanding the Use of Silicone Gels for Nonhermetic Plastic Packaging," *IEEE CHMT* **12** (4) (December 1989).
104. M. J. Loboda *et al.*, "Manufacturing Semiconductor Integrated Circuits with Built-in Hermetic Equivalent Reliability," Proceedings of the 1996 IEEE ECTC (Orlando, FL, May 1996).
105. Air Force Research Laboratory contract F29601—Avanteco.
106. "Highly Integrated Packaging and Processing," Air Force Research Laboratory contract F29601-92-C-0137, Subtask 03-07.
107. F. Miller, "Space Qualifiable, Corrosion Resistant, Near Hermetic Plastic Packages," Air Force Research Laboratory contract F29601- 97-C-0046.
108. M. Merker, *et al.*, "Rad-Pak Radiation Shielding for ICs at the Package Level," Air Force Weapons Laboratory Report no. AFWL-TR-83-117 (April 1984).
109. A. P. Schmid, "Feasibility of Rad-Pak for VHSIC Packages," Air Force Weapons
110. Laboratory Report no. AFWL-TR-86-128 (April 1988).
111. A. P. Schmid *et al.*, "Fabrication and Testing of Rad-Pak IC Packages," Air Force Weapons Laboratory Report no. AFWL-TR-86-25 (April 1988).
112. Space Electronics, Inc., San Diego, CA, http://www.spaceelectronics.com/SpaceProd/Technologies/RadCoat.html.
113. D. G. Mavis, "Integral Shielding of Multichip Modules of Natural Space Reaiation Environments," Defense Nuclear Agency Report no. DNA-TR-96-18 (Mission Research Corporation through Air Force Research Laboratory June 1996).
114. S. Patel and I. Burgess, "Integrated Scan Techniques Ease Chip and Board Tests," *EDN* **41** (24) 129–142 (21 November 1996).
115. T. Storey, "Testing MCMs with Boundary Scan," *EE-Evaluation Eng.* (September 1994).
116. L. Peters, "A Better Method for Testing CMOS ICs," *Semiconductor Int.* (November 1991).
117. S. Ehlscheid, "A Practical method to Increase Test Coverage Using IDDQ," *EE-Evaluation Eng.* (August 1995).
118. *Plug and Play ISA Specification*, Microsoft and Intel Corporations, Version 1.0a (1994).
119. M. Wilinson, "Microsystem Integration Levels under Question," *Electron. Eng. Times*, 15 June, 1998.
120. D. C. Jiles, *Introduction to the Electronic Properties of Materials* (Chapman and Hall, New York, 1994).
121. M. Little and J. Grinberg, "The 3-D Computer: An Integrated Stack of WSI Wafers," in *Wafer Scale Integration*, edited by E. Swartzlander (Boston, MA, Kluwer Academic, 1989).